7E4240

B. Tech. VII Semester (Main/Back) Examination 2013

COMPUTER ENGINEERING # 7CS4

COMPUTER AIDED DESIGN FOR VLSI

Time : 3 Hours **Min. Passing Marks : 24** **Maximum Marks : 80**

Instruction to Candidates :

*Attempt any **five** questions, selecting **one** question from **each** unit. All questions carry **equal** marks. (Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.)*

Unit–'I'

1. (*a*) Describe computer-aided synthesis and optimization. **[8]**

   (*b*) What is cell based design style? Explain in terms of library binding. **[8]**

OR

1. (*a*) What is Moore's law, locate the present status on it, predict its validity in near future. **[8]**

   (*b*) What are the circuit models? Discuss the classification of models on the basis of levels and views. **[8]**

Unit–'II'

2. (*a*) What is binary decision diagram? Explain ROBDD algorithm with an example. **[8]**

   (*b*) What are distinctive features of HDL. **[8]**

OR

2. (*a*) How do you differentiate between structural and behavioural HDL? Explain with example. **[8]**

   (*b*) Write a technical note on: **[8]**

   (i) Sequencing graph

   (ii) Hierarchical graph.

Unit–'III'

3. (*a*) What is ill-posed constraint graph? Give one example in which ill-posed sequencing graph can be converted in to well-posed graph. **[8]**

   (*b*) Give the ASAP and ALAP algorithm and explain with an example. **[8]**

OR

3. Write technical note on the following:

   (i) Force directed scheduling **[4]**

   (ii) Multiprocessor scheduling **[4]**

   (iii) Heuristic scheduling **[4]**

   (iv) Scheduling constraints and resources. **[4]**

Unit–'IV'

4. (*a*) Explain the testability properties on two-level logic cover positional cube notation. **[8]**

   (*b*) Explain the exact logic minimization and principle for logic operation. **[8]**

OR

4. (*a*) Explain the functions with multi volume inputs and list oriented manipulation. **[8]**

   (*b*) What are combinational circuits and sequential circuits. **[8]**

Unit–'V'

5. (*a*) Explain clock routing and power routing. **[8]**

   (*b*) What is placement? What are the different levels of placement. Explain in detail. **[8]**

OR

5. (*a*) Explain floorplanning and stimulated annealing in detail. **[8]**

   (*b*) Explain left-edge algorithm in detail. **[8]**