5E 5102

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B. Tech. V Semester (Main/Back) Examination, Dec., 2014

COMPUTER SCIENCE & ENGINEERING # 5CS2A

DIGITAL LOGIC DESIGN

Time : 3 Hours | Min. Passing Marks : 24 | Maximum Marks : 80

Instruction to Candidates :

Attempt any five questions, selecting one question from each unit. All questions carry equal marks. (Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.)

Unit-I

1. (*a*) Explain the concept of Computer Aided Design (CAD) in modern digital system with the help of a flow diagram. [8]

   (*b*) Write VHDC code for 4 bit Serial In Serial Out (SISO) shift register by using structural modeling only. [8]

OR

1. (*a*) Write VHDL code for rising edge J-K flip flop by using behavioral modeling. [8]

   (*b*) Describe the following terms in connection with Computer Aided Design (CAD) process :

   (*i*) Design entry

   (*ii*) Simulation of a design

   (*iii*) Synthesis of a design

   (*iv*) Optimization of a design. [8]

Unit-II

2. What is simulation and synthesis? Draw timing simulation of VHDL code given below :

```
Entity logic is
Port (x1, x2, x3: in bit;
      f: out bit);
end logic;
architecture logic 1 of logic is
begin
    f<= ((not x1 and not x2 and x3) or (x1 and x2 and
    not x3) or (x1 and not x2 and x3)
        or (x1 and not x2 and x3));
end logic 1;
```

[8]

OR

2. (*a*) Explain any five VHDL statements using an example for each. [8]

   (*b*) Write two differences (also support with any example for explanation) between package and entity. [8]

Unit-III

3. (*a*) What do you understand by clock skew? How can it be avoided by clock synchronization? [10]

   (*b*) Write the difference between Moore and Mealy machines. [6]

OR

3. Discuss the concept and working principle of following:

   (*i*) ROM

   (*ii*) FPGA

   (*iii*) PLA

   (*iv*) PLD [4×4 = 16]

Unit-IV

4. What is meant by race free assignment? Explain the procedure of state reduction of incompletely specified machines with suitable examples. [16]

OR

4. (*a*) Differentiate between :

   (*i*) Transition table vs flow table

   (*ii*) Critical vs Non critical races

   (*iii*) Internal state vs. total state

   (*iv*) Stable vs unstable [4×2 = 8]

   (*b*) What do you understand by dynamics hazards? Explain with example. [8]

Unit-V

5. Why do we use FPGA kits? Explain logic elements and programmability. [16]

OR

5. Write short notes on :

   (*a*) Flash memory

   (*b*) Look up table technology. [8×2 = 16]