5E3253

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# 5E3253

**B. Tech. (Sem. V) (Main/Back) Examination, December - 2013**
**Computer Science**
**5CS2 Digital Logic Design**

Time : **3** Hours] [Total Marks : **80**
[Min. Passing Marks : **24**

*Attempt any five questions. Selecting one question from each unit. All questions carry equal marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used / calculated must be stated clearly.*

Use of following supporting material is permitted during examination.
*(Mentioned in form No. 205)*

1. NIL 2. NIL

## UNIT - I

1 (a) Write a VHDL code for J-K flip flop. 8

(b) Describe the hardware description language. Discuss the data type and operations in VHDL. 8

**OR**

1 Describe look ahead carry adders with its VHDL code. Also draw its simulation waveform. **16**

## UNIT - II

2 (a) Explain the difference between concurrent and sequential statements. 8

(b) Write a VHDL code for 4 bit counter using D flip flop with the help of IF GENERATE scheme. 8

**OR**

2 Write a short note on following :
(i) Use of VHDL in simulation and synthesis
(ii) Packages and use clauses in VHDL. **16**

## UNIT - III

3 (a) ASM (Algorithm State Machine) is a controller for logic design of a digital system and is regarded as a hardware algorithm. Show the general model of ASM and explain the working of each functional block. 8

(b) Describe the one hot encoding method with its excitation table. 8

**OR**

3 (a) Draw a synchronous sequential circuit with a single input line X and a single output line Z so as to produce an output Z=1 whenever an input symbol completes as sequence of 4 identical input bits. The output is to be 0 otherwise. Also write its Boolean function expression. 6

(b) Describe the functioning of PLA with a block diagram. 4

(c) Discuss the difference between Mealy and Moore machine. 6

## UNIT - IV

4 (a) Explain the design procedure for asynchronous sequential circuit with suitable example. 8

(b) Explain the static and essential hazards in digital circuit. 8

**OR**

4 Design a asynchronous sequential circuit with two input T and C. The output attains a value of 1 when T = 1 and C moves from 1 to 0. Otherwise the output is 0.

(a) Draw the state diagram

(b) Draw the flow table

(c) Using implication table reduce the flow table

(d) Obtain transition table. 16

## UNIT - V

5 (a) Which are the programmable elements of FPGA module ? Explain the function of each of them in detail. 8

(b) Describe the case study of Altera stratix. 8

**OR**

5 Write short note on :
(a) Technology mapping in FPGA
(b) SRAM 16

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