4E2110

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4E2110

B.Tech. IVth Semester (Main/Back) Examination, June - 2010

Electrical Engineering

4EE2 Digital Electronics

Time : 3 Hours **Maximum Marks : 80**

Min. Passing Marks : 24

Instructions to Candidates:

*Attempt overall **five questions** selecting **one question** from **each unit**. All questions carry **equal marks**. (Schematic diagrams must be shown wherever necessary. Any data you feel missing may suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.)*

Unit - I

1. a) Convert the decimal number 250.3 to base 3, base 4, base 7 and base 16. **(8)**

   b) Perform the subtraction with the following binary numbers using 2's complement and 1's complement method. **(4+4)**

   i) 01000 - 01001

   ii) 0011.1001 - 0001.1110.

2. a) Represent the decimal number 8620 in BCD, excess - 3 code, 2421 code and binary number. **(8)**

   b) Determine the odd parity bit generated when the message consists of the ten decimal digits in the 8, 4, -2, -1 code **(8)**

Unit - II

3. a) **Simplify the following using boolean algebra** **(8)**

   i) $\left(\overline{\overline{CD}+A}\right)+A+CD+AB$

   ii) $(A+C+D)(A+C+\overline{D})(A+\overline{C}+D)(A+\overline{B})$

   b) Minimize the logic function using K-map and realize using NAND/NOR gates.

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$F(A, B, C, D) = \Pi M(1,2,3,8,9,10,11,14).d(7,15)$. **(8)**

Unit - III

5. a) Explain the working of CMOS NAND and NOR gates. **(8)**

b) Explain the working of ECL NOR gate. **(8)**

6. a) Draw and explain the circuit diagram of a TTL-NAND gate with to tempole output.

b) Write short notes on the following:

i) Propagation delay.

ii) Power dissipation.

iii) Fan out.

iv) Noise immunity. **(16)**

Unit - IV

7. a) Implement the expression using a multiplexer. **(8)**

$F(A, B, C, D) = \sum m(0, 2, 3, 6, 8, 9, 12, 14)$.

b) Draw and explain BCD adder using binary adder. **(8)**

8. a) Implement the expression using 4 to 16 line decodes.

$F = \sum m(1, 2, 4, 7, 8, 11, 12, 13)$. **(8)**

b) Design and draw a full adder with NAND gates using K-map. **(8)**

Unit - V

9. a) Design a 3-bit synchronous counter using J-K Flip-Flops. **(8)**

b) What is race-around condition and how it can be eliminated? **(8)**

10. a) Realise J-K Flip-Flop using S-R Flip-Flop. **(8)**

b) Explain and draw a 4 - bit bi-directional shift register. **(8)**