B. Tech. (Sem. VIII) (Main/Back) Examination, April/May - 2011
Electronics & Comm.
8EC4.2VHDL

Time : **3** Hours]   [Total Marks : **80**
[Min. Passing Marks : **24**

Attempt any five questions, selecting one question from each unit. All questions carry equal marks. (Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly, Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. *(Mentioned in form No. 205)*

1. _____ **Nil** _____   2. _____ **Nil** _____

UNIT-I

1 (a) Draw the schematic for ASIC design flow and explain every step in brief.

       10

(b) Explain the history of various hardware description language.

       6

OR

2 (a) Explain the data flow and structural modeling scheme using suitable example.

       10

(b) Explain the following :
  (i) Entity decleration
  (ii) Architecture deleration.

       3+3

UNIT-II

3   (a)   Explain multiplexer synthesis using Shannon's expansion and prove Shannon's expansion theorem.

                                10

    (b)   Write VHDL code 2-to-1 multiplexer specifed using if-then-else statement.

                                6

OR

4   Write hierarchical code for 16-to-1 multiplexer using structural modeling.

                                16

UNIT-III

5   (a)   Write VHDL code for D flip-flop using a wait untill statement.

                                8

    (b)   Explain the comparison of level sensitive and edge trigged D-storage elements, with the help of suitable timing diagram.

                                8

OR

6   (a)   Write VHDL code for a four-bit up counter.

                                8

    (b)   Draw the schematic diagram of parallel access shift register and explain it.

                                8

UNIT-IV

7   (a)   Draw the block diagram for MEALY-TYPE FSM and explain it using state diagram, state table, state assigned table.

                                10

    (b)   Compare Mealy and Moore type FSM.

                                  6

OR

8 (a) Write VHDL code for serial adder.

10

(b) Explain vending machine using timing diagram and block diagram.

6

UNIT-V

9 (a) Explain the schematic diagram of a $2^m \times n$ SRAM block and explain it.

8

(b) Draw the schematic diagram for the datapath circuit for the sort operation.

8

OR

10 Explain the following :
(a) Clock synchronization
(b) Design example of divider.

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