B. Tech Second Year : 3rd Semester

Electronic Devices & Circuits, Jan., 2012

(FOR 3EC2 BRANCH OF ENGINEERING)

Times : 3 Hours | **Min. Passing Marks : 24** | **Total Marks : 80**

*Attempt overall **five** questions in all. Schematic diagrams must be shown wherever necessary. Any data you feel missing may suitably be assumed and stated clearly.*

Unit–'I'

1. **(a)** Describe the conductivity and mobility for intrinsic semiconductor. **[8]**

   (b) Find the conductivity of intrinsic germanium at 300°K. If donor type impurity is added to the extent of 1 impurity atom in 10^7 germanium atoms, find the conductivity. Given that n_i at 300°K is $2.5 \times 10^{13}/cm^3$ and μ_n and μ_p of germanium are 3800 and 1800 cm^2/v-s respectively. **[8]**

OR

1. **(a)** What is Hall effect, how it is useful for measuring various parameters of semiconductor? **[8]**

   (b) What do you mean by Fermi level? Derive the expression for fermi level and sketch the position in case of intrinsic, p-type and n-type semiconductor. **[8]**

Unit–'II'

2. **(a)** Draw and explain the working of DC inserter circuit. **[8]**

   (b) What do you mean by clipper circuit? The sinusoidal input given to below circuit, what will be the output : Fig.1? **[8]**

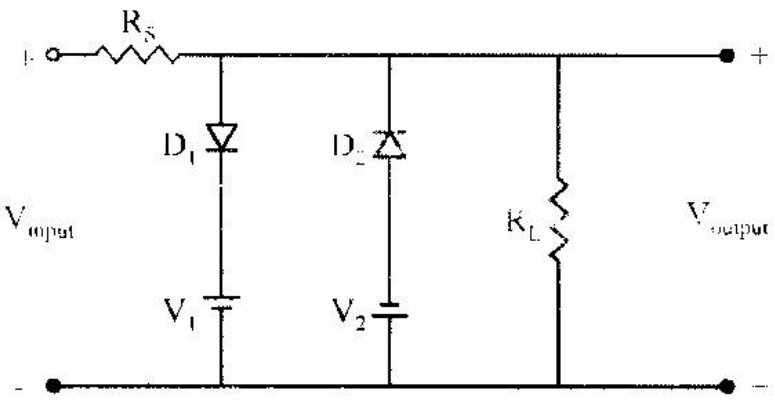

Fig. 1 **[8]**

OR

2. **(a)** Describe the importance of load line concept used in electronic circuits. **[8]**

   (b) Explain the effect of negative resistance region in the V-I characteristic of UJT, also give its applications. **[8]**

Unit–'III'

3. **(a)** Explain Ebers-Moll model of transistor. **[8]**

   (b) Draw and explain the working of transistor as an amplifier. **[8]**

OR

3. **(a)** Write the steps for testing of transistors by digital multimeter.
   (i) lead identification (base, collector, emitter)
   (ii) type of transistor (npn or pnp)
   (iii) it is good or not. **[10]**

   (b) Write short notes on stabilization techniques for transistor circuit used for different applications. **[6]**

Unit–'IV'

4. **(a)** It is required to operate the JFET shown in fig. 2 at $V_{GS} = -1$ V, $V_{DS} = 4$ V and $I_{DS} = 1$ mA. Determine:
   (i) value of R_D and R_S
   (ii) voltage gain
   (iii) Input and output resistance

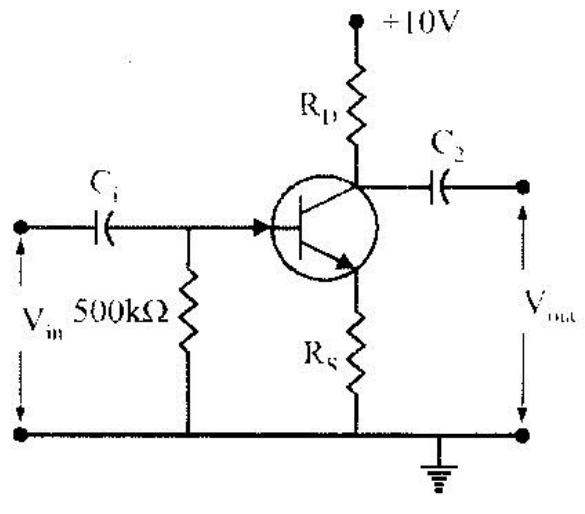

Fig. 2 **[8]**

   (b) Derive various parameters of JFET soft bias configuration useful in using different applications. **[8]**

OR

4. **(a)** Draw and explain the construction and operation of enhancement MOSFET. **[8]**

   (b) Write various techniques used for handling MOSFET in laboratory. **[8]**

Unit–'V'

5. Write short notes on the following : (any two)
   (a) Role of bootstraping in darlington pair
   (b) Emitter follower
   (c) Cascading transistor amplifiers. **[16]**