8E5004

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B.Tech. (Sem.VIII) (Main/Back) Examination - 2013
Computer Science
8CS4.1 Hardware Testing and Fault Tolerance (Elective)

Time : 3 Hours

[Total Marks : 80
[Min. Passing Marks : 24

Instructions to Candidates :
Attempt any five questions selecting one question from each unit. All questions carry equal marks.
Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed
and stated clearly. Units of quantities used/calculated must be stated clearly.

UNIT - I

1. (a) Explain how physical defects can be modeled as faults.
   (b) What is stuck-at-faults? Explain Bridging fault and Transient faults.   7
   9

OR

1. (a) What is exhaustive testive? Explain Pseudo-Random testing?
   (b) Explain the concept of test pattern generation and fault coverage.   8
   8

UNIT - II

2. What is VLSI design? Explain various methods used for the representation of VLSI design and their descriptions. 16

OR

2. (a) Explain VLSI desing flow and importance of simulation and fault simulation.
   (b) Describe parallel and deductive fault simulation.   10
   6

UNIT - III

3. (a) Explain D algorithm and its advantages.
   (b) Describe the methods for testing sequential circuits.   7
   9

OR

3. (a) Explain functional and deterministic ATPG for sequential circutis and various challenges associated with this.

   (b) Write short note on boundary scan testing.   10
   6

UNIT - IV

4. What is built in self test? Explain circular BIST architecture in detail.

OR   16

4. (a) Explain the concept of response compaction.
   (b) What are random pattern-resistant faults? Explain memory BIST in detail.   7
   9

UNIT - V

5. Describe the following terms related to hardware fault tolerance.
   (a) Failure Rate
   (b) Mean time to failure
   (c) Reliability

OR   5+6+5=16

5. (a) Explain different kinds of redundancy schemes for fault tolerance.
   (b) Write short note on parity code.

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4