C 44422 (Pages : 2) Name.....

Reg. No.....

SEVENTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION, JUNE 2013

EC 09 703 – ANALOG AND MIXED MOS CIRCUITS

(2009 Scheme – Supplementary)

Time : Three Hours Maximum : 70 Marks

Part A

Answer **all** *questions.*

Each question carries 2 *marks.*

I. (a) What is charge feed through effect?

(b) Draw the schematic of a simple MOS current sink.

(c) Define Stability.

(d) Draw the Series and Parallel resistance realization of switched capacitor circuits.

(e) Define Lock range of a PLL.

(5 × 2 = 10 marks)

Part B

Answer any **four** *questions.*

Each question carries 5 *marks.*

II. (a) What are the limitations of Passive resistors in monolithic technology? Explain.

(b) Derive the output Resistance R_0 of a cascode current mirror.

(c) Explain the operation of any one high gain amplifier architecture.

(d) Explain the design steps in single stage operational amplifier design.

(e) Explain the non-ideal effects of PLL.

(f) Explain the operation of a Sample and Hold circuit.

(4 × 5 = 20 marks)

Part C

Answer **all** *questions.*

III. (a) Explain the parasitics and limitations of CMOS Technology.

Or

(b) Discuss in detail about the Band gap reference circuit.

Turn over

IV. (a) Derive the frequency response of a Differential amplifier.

Or

(b) With necessary derivation and circuit schematic, explain the operation of a Gilbert Multiplier Cell.

V. (a) (i) Explain the design of two stage operational amplifier.

(ii) What are the advantages of cascode configuration? Explain.

Or

(b) With necessary derivation, explain the switched capacitor integrator.

VI. (a) With block diagram, explain the operation of a Phased Locked Loop.

Or

(b) Explain the operation of any one high speed comparator architecture.

(4 × 10 = 40 marks)

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