SEVENTH SEMESTER B.TECH DEGREE EXAMINATION, 2012

EC09 703 Analog and Mixed MOS Circuits

Time: Three hours **Maximum:70 marks**

Part A

*Answer **all** questions*

1. Describe flicker noise in MOSFET.
2. Calculate the small signal output resistance for a simple current mirror if output current is 100μA and channel length modulation parameter is 0.04.
3. Draw the circuit of CMOS source follower. Mention its advantages and disadvantages.
4. Define PSRR and common-mode input range of an opamp.
5. Describe a first order switched capacitor filter.

(5 x 2 = 10 marks)

Part B

*Answer **any four** questions*

6. Draw large signal model for the MOS transistor. Explain the reason for existence of various capacitances in the model.
7. What is meant by weak inversion region in a MOS transistor? Explain with the help of transconductance characteristic of MOSFET.
8. Draw the large signal transconductance characteristics of a CMOS differential amplifier. Derive necessary equations to draw the characteristics**.**
9. Derive unity gain bandwidth in a two stage CMOS opamp.
10. Draw the circuit of CMOS Analog Multiplier and Explain.
11. Explain fully differential sample-and-hold circuit that eliminates clock feedthrough and charge injection problems.

(4 x 5 = 20 marks)

Part C

*Answer **all** questions*
Each question carries 10 marks

12. (a) Draw the circuit of cascode current sink and its equivalent small signal model. Calculate the output resistance and minimum output voltage, while maintaining all the devices in saturation. (10 marks)

Or

(b) With neat sketch explain bandgap voltage reference. Prove that this circuit provides a reference voltage that has very little dependence on temperature and power supply. (10 marks)

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13. (a)(i) Draw the circuit of the CMOS differential amplifier with active load and current source(current mirror) biasing. Also draw the small signal equivalent circuit of the differential amplifier under difference mode and common mode operation.

(4 marks)

(ii)Find the maximum input common mode voltage, v_{ICmax} and minimum input common mode voltage, v_{ICmin} of the n-channel differential amplifier (differential amplifier with active load and current mirror biasing). Assume that all the transistors have W/L of 10µm/1µm and they are in saturation. Assume Iss= 10µA, $V_{DS5}(sat)=0.2$, $\mu_n C_{ox}=90\mu A/V^2$, $\mu_p C_{ox}=45\mu A/V^2$, V_{TP}= -0.85V, V_{TN}=0.55V, V_{DD}=4V, V_{SS}=0

(6 marks)

Or

(b) Derive the expression for voltage gain and output resistance in a cascode amplifier.What are the advantages of cascode amplifier? (10 marks)

14. (a) Design the currents and W/L values of the two stage CMOS opamp to satisfy the following specifications $V_{DD}=-V_{SS}=2.5V$, Slew Rate $\geq$ 10V/µs GB= 5MHz, C_L=10pF, -1V $\leq$ ICMR $\leq$ 2V. Assume model parameters $\mu_n C_{ox}=110\mu A/V^2$, $\mu_p C_{ox}=50\mu A/V^2$ V_{TN}=0.7V, V_{TP}= -0.7V, λ_N =0.04V^{-1}, λ_P=0.05V^{-1}, Also the transistors in the current mirror load are perfectly matched and output pole is assumed to be placed at 2.2 times GB so that Compensating capacitor can be assumed as 0.22 C_L. (10 marks)

Or

(b)(i) Derive expression for switched capacitor resistor. Describe the circuit with necessary waveforms.

(4 marks)

(ii)Explain two arrangements of switched capacitor transresistor circuits that are independent of capacitor parasitics. Using these circuits design a noninverting and inverting switched capacitor voltage amplifiers that is independent of parasitic capacitors.

(6 marks)

15. (a) (i) Explain the steps to design a CMOS comparator. (6 marks)

(ii) Describe clocked comparator (4 marks)

Or

(b)(i) Explain charge-pump PLL with neat sketches. (6 marks)

(ii) Briefly explain the non-ideal effects seen in PLL. (4 marks)

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