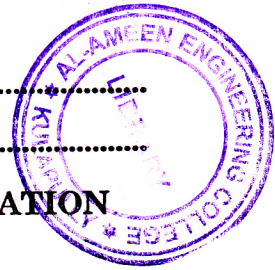


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Name.....

Reg. No.....



**SIXTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION
MAY 2012**

EC/PTEC 09 601—VLSI DESIGN

(2009 Admissions)

Time : Three Hours

Maximum : 70 Marks

Part A

*Answer all questions.
Each question carries 2 marks.*

1. Define Body Effect.
2. What is Charge Sharing ?
3. What are the types of diffusion ?
4. What is LOCOS ?
5. Compare CMOS and BJT.

(5 × 2 = 10 marks)

Part B

*Answer any four questions.
Each question carries 5 marks.*

6. Briefly explain short and narrow channel effects in MOS transistor.
7. Explain the estimation of interconnect parasites.
8. Explain the operation of carry bypass adder.
9. Write a note on testing of VLSI circuits.
10. What is a photoresist ? Explain its types.
11. Explain the twin-tub process.

(4 × 5 = 20 marks)

Part C

*Answer all questions.
Each question carries 10 marks.*

12. (a) Discuss in detail about the various second order effects in MOS.

Or

- (b) Derive an expression for the saturation current of a CMOS inverter in its various region of operation.

13. (a) With transistor-level schematic explain the operation of a carry select adder.

Or

- (b) (i) Draw the schematic of a 4×4 array multiplier using static CMOS logic and explain its operation.

(6 marks)

- (ii) Explain any *one* method test generation.

(4 marks)

Turn over

14. (a) Discuss in detail about the Ion Implantation.

Or

(b) Discuss in detail about the etching process and its types.

(10 marks)

15. (a) Discuss in detail about :

(i) Schottky contacts.

(ii) Implanted ohmic contacts.

(iii) Alloyed contacts.

(iv) Refractory metal contact.

(4 × 2½ = 10 marks)

Or

(b) (i) Discuss in detail about the Lambda based design rules.

(6 marks)

(ii) Draw the layout of a CMOS inverter.

(4 marks)

(4 × 10 = 40 marks)