FOURTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION MARCH/APRIL 2012

EC 09-405/PTEC 09 404—COMPUTER ORGANIZATION AND ARCHITECTURE

(2009 Admissions)

Time : Three Hours   Maximum : 70 Marks

Part A

Answer all questions.

1. Registers R1 and R2 of a computer contain the decimal values 1200 and 4600. What is the effective address of the memory operand in each of the following instructions ?

    (a) Load 20(R1), R5.

    (b) Add → (R2), R5.

2. What are the most common fields found in an instruction format ?

3. Define Memory Density and Memory Access time.

4. What is an Interrupt ?

5. What is a stack ?

(5 × 2 = 10 marks)

Part B

Answer any four questions.

6. Briefly explain the *four* methods of control organization.

7. Write a note on Multilevel Memories.

8. Explain the shared Bus system.

9. Write a note on Virtual and Cache Memories.

10. Explain Parallel Processing.

11. With a suitable example, explain the Subroutine.

(4 × 5 = 20 marks)

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Name..

Reg. No...

FOURTH SEMESTER B.TECH. (ENGINEERING) DEGREE EXAMINATION MAY 2012

EC 09 406/PTEC 09 405—SOLID STATE DEVICES

Time : Three Hours

Maximum : 70 Marks

Part A

Short answer questions.

1. What is the significance of Fermi-Dirac function ?
2. What is avalanche breakdown ?
3. Why is BJT called current controlled device ?
4. What is kirk effect ?
5. What is strong inversion in MOSFET ?

(5 × 2 = 10 marks)

Part B

Answer any **four** *questions.*

6. Derive the expression for charge concentrations of semiconductor doped with pentavalent impurity.
7. Derive the expression for drift current in semiconductors.
8. Derive the expression for built in potential of a graded PN junction.
9. With circuit diagram explain and write the expressions for terminal currents of *p-n-p* BJT.
10. Explain the short-channel effects in MOSFET.
11. Explain the concept of threshold voltage in N-MOSFET and P-MOSFET.

(4 × 5 = 20 marks)

Part C

12. (a) Derive the continuity equation.

Or

(b) Derive the expression for Fermi-level in intrinsic semiconductor.

13. (a) Explain Schottky effect and derive an expression for change in potential barrier due to image charge and applied bias voltage.

Or

(b) Draw the structure of GaAs isotope diodes and explain its characteristics.

14. (a) Draw the Eber-Moll model for BJT and write the analytical expressions for transistor characteristics.

Or

(b) Draw the structure of JFET and explain its operation.

15. (a) Explain the working and characteristics of *n*-channel, depletion MOSFET with diagrams.

Or

(b) Explain the working of floating gate MOSFET with diagram.

(4 × 10 = 40 marks)