[05–3105]

III/IV B.E. DEGREE EXAMINATION.

First Semester

Electrical and Electronics Engineering

Elective I — COMPUTER ARCHITECTURE AND ORGANIZATIONS

(Common for EEE, ECE, E&IE)

(Effective from the admitted batch of 2003-2004)

Time : Three hours Maximum : 70 marks

First question is compulsory.

Answer any FOUR from the remaining.

All questions carry equal marks.

1. Write briefly on the following: $(7 \times 2 = 14)$

   (a) RTL

   (b) Instruction Cycle

   (c) Convert the arithmetic expressions from infix to reverse Polish notation

   A*B+A*(B*D+C*E)

   (d) Indexed addressing mode

   (e) I/O processor

   (f) Locality of reference

   (g) Loosely coupled systems.

2. (a) Show the hardware that implements the following statement. Include the logic gates for the control function and a block diagram for the binary counter with a count enable input.

$$xyT_0 + r + y'T_2 : AR \leftarrow AR + 1$$

(b) Consider the following register transfer statements for two 4-bit registers R_1 and R_2.

$$xT : R_1 \leftarrow R_1 + R_2$$

$$xT : R_1 \leftarrow R_2$$

Every time that variable T = 1, either the content of R_2 is added to the content of R_1 if $x = 1$, or the content of R_2 is transferred to R_1 if $x = 0$. Draw a diagram showing the hardware implementation of the two statements. Use block diagrams for the two 4-bit registers, a 4-bit adder, and a quadruple 2-to-1-line multiplexer that selects the inputs to R_1. In the diagram, show how the control variables x and T select the inputs of the multiplexer and the load input of register R_1.

3. (a) A digital computer has a memory unit with a capacity of 16,384 words, 40 bits per word. The instruction code format consists of six bits for the operation part and 14 bits for the address part (no indirect mode bit). Two instructions are packed in one memory word, and a 40-bit instruction register IR is available in the control unit. Formulate a procedure for fetching and executing instructions for this computer.

(b) Show the contents in hexadecimal of registers PC, AR, DR, IR and SC of the basic computer when an ISZ indirect instruction is fetched from memory and executed. The initial content of PC is 7FF. The content of memory at address 7FF is EA9F. The content of memory at address A9F is OC35. The content of memory at address C35 is FFFF. Give the answer in a table with five columns, one for each register and a row for each timing signal. Show the contents of the registers after the positive transition of each dock pulse.

4. (a) A computer has 32-bit instructions and 12-bit addresses. If there are 250 two-address instructions, how many one address instructions can be formulated?

(b) How many times does the control unit refer to memory when it fetches and executes an indirect addressing mode instruction if the instruction is

(i) a computational type requiring an operand from memory;

(ii) a branch type.

5. (a) The microprogrammed control organization has the following propagation delay times. 40 ns to generate the next address, 10 ns to transfer the address into the control address register, 40 ns to access the control memory ROM, 10 ns to transfer the microinstruction into the control data register and 40 ns to perform the required microoperations specified by the control word. What is the maximum clock frequency that the control can use? What would the clock frequency be if the control data register is not used?

(b) Explain how the mapping from an instruction code to a microinstruction address can be done by means of a read-only memory. What is the advantage of this method?

6. (a) Describe in words and by means of a block diagram how multiple matched words can be read out from an associative memory.

(b) Obtain the Boolean function for the match logic of one word in an associative memory taking into consideration a tag bit that indicates whether the word is active or inactive.

7. (a) A DMA controller transfer 16-bit words to memory using cycle stealing. The words are assembled from a device that transmits characters at a rate of 2400 characters per second. The CPU is fetching and executing instructions at an average rate of 1 million instructions per second. By how much will the CPU be slowed down because of the DMA transfer?

(b) Give at least six status conditions for the setting of individual bits in the status register of an asynchronous communication interface.

8. Write short notes on the following:

(a) Segmentation

(b) How many switch points are there in a crossbar switch network that connects p processors to m memory modules?

(c) Snoopy Cache controller.