[07 – 2101]

II/IV B.Tech. DEGREE EXAMINATION.

First Semester

Computer Science and Engineering

ELECTRONICS — I

(Common with IT and Dual Degree Program in SE/IT)

(w.e.f admitted batch of 1999-2000 and after batches)

Time : Three hours Maximum : 70 marks

Question No. 1 is compulsory.

Answer any FOUR from the remaining.

All questions carry equal marks.

Answer all parts of any question at one place.

1. Answer the following :

(a) What is meant by majority and minority charge carriers? What are the majority charge carries in n-type material?

(b) What is diffusion current? What it is observed and also write equation for hole diffusion current?

(c) What is the use of varactor diode? Draw its symbol.

(d) Compare PNP and NPN transistors.

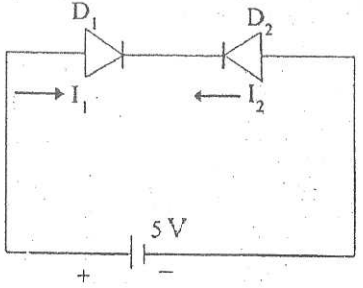
(e) Write the expressions for stability factor of self biasing and collector to base bias.

(f) Compare BJT and FET.

(g) Specify the rectifier efficiency for
(i) Full wave rectifier
(ii) Half wave rectifier and
(iii) Bridge rectifier

2. (a) Draw and explain the formation of depletion region in an open circuited p-n diode and also explain how depletion region will vary in forward biasing and reverse biasing.

(b) Find the voltage drop across each of the silicon diode as shown in figure at room temperature. Assume that reverse saturation current flows in the circuit and the magnitude of reverse breakdown voltage is greater than 5 V.



3. (a) Clearly explain

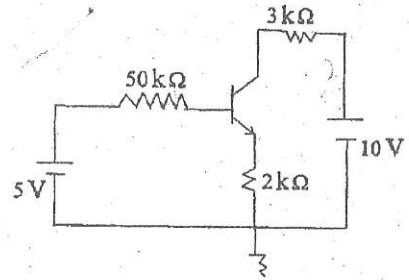
(i) Avalanche breakdown

(ii) Zener breakdown with neat diagrams.

(b) Draw the circuit of Zener voltage regulator. Explain its operation with neat characteristics and also derive the expressions for minimum and maximum values of source resistor for the Zener diode to work as a voltage regulator.

4. (a) Explain Early effect and its consequences in a BJT. Also draw the Embers Moll model of a PNP transistor.

(b) In the circuit shown, a silicon transistor with $\beta = 99$, $V_{BE} = 0.6\,V$ and $V_{CEsat} = 0.2\,V$ is used. Determine whether the transistor is operated in active region or in saturation region.



5. (a) With neat diagram and necessary equations, explain how the variations in V_{BE} is compensated with the variations in temperature.

(b) Design a self bias circuit using s_i transistor to achieve stability factor of 10, with the following specification. V_{CC} = 16 V, V_{BE} = 0.7 V, V_{CEO} = 8 V, I_{CQ} = 4 mA and $\beta = 50$.

6. (a) What are the requirement of FET biasing? Verify these requirements in source - self bias circuit.

(b) Draw the Drain characteristics of n channel J-FET amplifier with variations in VGS and VDS.

7. (a) Explain the operation of Full wave rectifier with input and output wave forms.

(b) In a full wave rectifier with capacitor filter, Show that ripple voltage is inversely proportional to the capacitance of capacitor and is proportional to the load current. Calculate the ripple voltage when C = 100 μF, $I_{DC} = 10\,mA$. The ac I/P is $V_m \sin 3/4t$.

8. (a) Draw the circuit of two stage R-C coupled JFET amplifier and explain its working.

(b) If six identical R-C coupled amplifiers are cascaded each having f_L = 100Hz. Determine the overall f_L.