7. (a) A 16 K*4 memory uses coincident decoding by splitting the internal decoder into X – selection and Y – selection.

(i) What is the size of each decoder, and how many AND gates are required for decoding the address?

(ii) Determine the X and Y selection lines that are enabled when the input address is the binary equivalent of 6,000.

(b) Using 64*8 ROM chips with an enable input, construct a 512*8 ROM with eight chips and a decoder.

8. (a) Derive the ROM programming table for the combinational circuit that squares a 4 - bit number. Minimize the number of product terms.

(b) Explain about Universal Shift Registers.

[07 – 2115]

II/IV B.Tech. DEGREE EXAMINATION.

First Semester

Computer Science Engineering

DIGITAL LOGIC DESIGN

(Common with IT and Dual Degree Programme in SE/IT)

(Effective from the admitted batch of 2006–2007)

Time : Three hours Maximum : 70 marks

Question No. 1 is compulsory

Answer any FOUR questions from the remaining.

All questions carry equal marks.

Answer ALL parts of any questions at one place.

1. (a) What is the largest binary number that can be expressed with 16 bits? What are the equivalent decimal and hexadecimal numbers?

   (b) Draw the Negative logic OR gate and derive the truth table for negative logic OR gate.

   (c) Explain about Logic simulation.

(d) Explain about 4 – to – 1 multiplexer.

(e) What is the main difference between an initial statement and an always statement in Verilog HDL?

(f) Explain about ring counter.

(g) Explain about FPGA.

2. (a) The solutions to the quadratic equation :

$x^2 - 11x + 22 = 0$ are $x = 3$ and $x = 6$. What is the base of the numbers?

(b) Perform subtraction on the given unsigned numbers using the 10's complement of the subtrahend.

3. (a) Find the complement of the following functions by applying DeMorgan's theorems.

(i) $F1 = x'yz' + x'y'z$

(ii) $F2 = x(y'z' + yz)$

(b) Derive Boolean Expressions for the 16 functions of two variables.

4. (a) Draw a logic diagram using only two-input NOR gates to implement the following function :

$F(A, B, C, D) = (A \oplus B)'(C \oplus D)$

(b) Find all the prime implicants for the following Boolean functions, and determine which are essential :

(i) $F(w, x, y, z) = \Sigma(0, 2, 4, 5, 6, 7, 8, 10, 13, 15)$

(ii) $F(A, B, C, D) = \Sigma(0, 2, 3, 5, 7, 8, 10, 11, 14, 15)$.

5. Design a combinational circuit that converts a four-bit Gray code to a four bit binary number.

(a) Implement the circuit with exclusive – OR gates.

(b) Using a case statement, write and verify a Verilog model of the circuit.

6. (a) Design a sequential circuit with two JK flip-flops A and B and two inputs E and F. If $E = 0$, the circuit remains i the same state regardless of the value of F. When $E = 1$ and $F = 1$, the circuit goes through the state transitions from 00 to 01, to 10, to 11, back to 00, and repeats. When $E = 1$ and $F = 0$, the circuit goes through the state transitions from 00 to 11, to 10, to 01, back to 00, and repeats.

(b) Design a four – bit binary synchronous counter with D flip – flops.