[07 – 2115]

II/IV.B.Tech. DEGREE EXAMINATION.

First Semester

Computer Science and Engineering

DIGITAL LOGIC DESIGN

(Common with I.T and M.S. Software Engineering and Information Technology)

(Effective from the admitted batch of 2006–2007)

Time : Three hours Maximum : 70 marks

The First question is compulsory.

Answer FOUR from the remaining questions.

Answer all parts of any questions at one place.

All questions carry equal marks.

1. (a) Convert $(F5.E)_{16}$ into decimal.

   (b) What is a binary code? List out different binary codes.

   (c) What do you mean by register?

   (d) Convert $f(A,B,C)=(A+B)(B+C)$ to standard sum of product form.

   (e) What is a repple counter?

(f) What is a latch? Give its working principle and truth table.

(g) What is memory? List out the different types of memories.

2. (a) Find the excess –3 code and its 9's complement for decimal number 392, 712, 452 and 920.

(b) What is logic gate? List out its various types with neat diagram.

3. (a) Implement the following Boolean function with NAND – NAND logic :

$$y = AC + ABC + \overline{A}BC + AB + D.$$

(b) Simplify the logic expression $y = A\overline{B} + AB + \overline{A}B$ using Karnaugh map.

4. (a) What is multiplexer and demultiplexer? Explain them with neat lable diagram?

(b) Explain 4×2 encode with neat diagram.

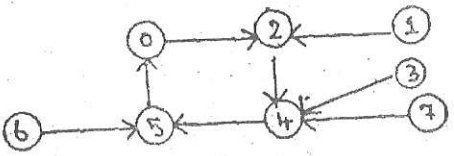
5. (a) Write the difference between a latch and flipflop.

(b) Design a combinational circuit that has four inputs and four outputs. The output generates the 2's complement of input binary number.

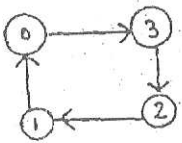
6. (a) Explain different types of registers with neat diagram.

(b) Design synchronous BCD counter with JK Flip–flops.

7. (a) Design the sequential circuit for the given state diagram using D flip–flop.



(b) Design the sequential circuit for the given state diagram using T flip flop.



8. (a) Explain the classification of Semi–conductor memories with neat lable diagram.

(b) What is PAL? How it differs from PROM and PLA.
