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B.E / B.Tech (Full Time) DEGREE END SEMESTER EXAMINATIONS, APR / MAY 2014

ELECTRICAL & ELECTRONICS ENGINEERING

Fourth Semester

EE 9252 Microprocessor and Microcontrollers

(Regulation 2008)

Time : 3 Hours Answer ALL Questions Max. Marks 100

PART-A (10 x 2 = 20 Marks)

1. State the purpose for which the signal 'Ready' is available in 8085?
2. What is 'register indirect addressing mode'? Illustrate with an example.
3. What is the length of Instruction Queue available in 8086?
4. Distinguish between reading a word data from even and odd addresses, in 8086?
5. Give an example instruction for bit oriented instructions of 8051? Which portion of its internal RAM memory is bit addressable?
6. What is the role for the B register in the micro-controller 8051?
7. Distinguish between memory mapped I/O and peripheral mapped I/O?
8. Frame the control word for setting the portC bit PC5 of 8255,without affecting other bits
9. What are the control signals normally employed when interfacing a typical successive approximation type ADC?.
10. Distinguish between the instruction PUSH PSW of intel8085 and that of µC 8051?

Part – B (5 x 16 = 80 marks)

11. i) A thumb wheel switch is connected as the input device, and two number of 7-segment LEDs connected through 7447 decoders form the output device. Both these are interfaced to µP 8085 through 8255 PPI. Assume suitable port connection. 8255 PPI itself is required to be connected following memory mapped I/O with address range of 9000- 9003H. Draw the hardware connections. Also write a program which reads in the BCD input from thumb wheel switch and displays the value of the sum of all natural numbers upto this input number, at the 7-segment displays?
ii) Same external hardware is now connected to a µC 8051; thumbwheel switch to port -1 and 7447 decoder ICs to the port-2. Write a program in µC 8051 assembly language, to perform the same task? (10 + 6) .

12. a) i) Write an assembly language program using µP 8085 for multiplication of given single byte numbers, using 'shift-and-add' method. Also write a program for division by 'repeated subtraction method'.
ii) Write an assembly language program using µC 8051 for performing multiplication and division of given two 8-bit numbers. Use MUL AB and DIV AB instructions respectively, after describing their operation. (8 + 8)

OR

b) i) Correct the mistake in the following delay subroutine of µP 8085. After correcting the program by adding required additional instructions, evaluate approximately the

count required to obtain a time delay of 7 msec. Assume a μP clock frequency of 3 MHz.

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Delay :     LXI  B, 16-bit count
Repeat :    DCX  B
            JNZ  Repeat
            RET.
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ii) Rewrite the delay subroutine for the generating the time delay of 7 msec, using the programmable interval timer 8253/ 8254 in mode-0. Use Counter-0 in BCD count mode. Assume a timer clock of 1 MHz and use 'Latch on count' feature.

iii) Using μC 8051 assembly language, write a time delay subroutine, which generates a delay of 7 msec. Use one of its internal timers in any suitable mode. Assume the crystal frequency to be 12 MHz. (5 + 6 + 5)

13. a) Along with a neat sketch of the architecture/ functional block diagram, describe the salient features of the microprocessor μP 8085 or microcontroller μC 8051 ?

OR

b) i) Show how would you interface a 4Kbyte EPROM and a 2Kbyte RAM to 8085. The memory map required is: 4K EPROM → A000h to AFFFh and 2K RAM → 8000h to 87FFh. You are permitted to use one 74138 IC, apart from one 7404 and one 7432 ?

ii) Draw the timing diagram showing fetching and complete execution of the μP 8085 instruction XRA M. Assume that this instruction is fetched from memory location 5432H? Discuss the role of reg A and register pair HL during the execution. (8 + 8)

14. a) Along with a neat sketch of the functional block diagram / architecture, describe the salient features available in the 16-bit μP 8086. Discuss the role of both BIU and EU. Also explain how the 20-bit physical address is evaluated jointly by these units, considering different cases of the addressing modes.

OR

b) Explain how a stepper motor can be controlled by employing either μP 8085 or μC 8051? Show the hardware connection diagram. Assume half step mode and write a program for deflecting the shaft by 10 full steps in either direction.

15. a) Write short notes on ANYTWO of the following:
i) Programmable Peripheral Interface – 8255,
ii) Keyboard / Display Interface -- 8279,
iii) Universal Synch. /Asynchronous Receiver/ Transmitter- 8251. (8 + 8)

OR

b) i) What are the interrupts available in the μP 8085? Specify if each of these is vectored/ non-vectored? In case of vectored interrupts, also specify the vector address values. Which of these are maskable? Also explain how would you mask the interrupts individually? What is the role of the instruction DI? Draw a schematic block diagram showing how the interrupts are handled by the internal hardware?

ii) What are the internal and external interrupts available in μC 8051? Give the vector locations for writing relevant Interrupt Service Routine. (10 + 6)