Roll No:						

B.E. (Full Time) Degree End Semester Examinations, NOV/ DEC 2012

ELECTRICAL & ELECTRONICS ENGINEERING,

Fourth Semester - (Regulation 2008)

EE 9252 MICROPROCESSORS AND MICRO CONTROLLERS

Time: 3 hr

Answer ALL questions

Max. marks: 100.

$PART - A (10 \times 2 = 20)$

- 1. What is the purpose for which the flag bit 'AC' is available in 8085?.
- 2. What is the purpose for which the signal $^{\circ}ALE'$ is available in μP 8085/ μC 8051?.
- 3. Show the decoding hardware necessary to interface a 4Kbyte sized EPROM to the 8085 with a required memory mapping of 3000 3FFF_H?
- 4. There is no explicit instruction for 'jumping if overflow flag is set' in μC 8051. How would you manage this, using the relevant bit oriented instruction available?.
- 5. Distinguish between the operation performed by the instructions: INR D and INX D?
- 6. What is the purpose for ICW1 of the programmable interrupt controller 8259?
- 7. What are the roles for the HL register pair of µP 8085?.
- 8. Discuss the operation performed by the 8051 instruction DIV AB. How does this instruction affect the overflow flag?
- 9. What is/are the instruction(s) available in μC 8051 to make reference to a look-up table included as a part of the program code?
- 10. What is the operation performed by the instruction 'PUSH PSW' in μ P 8085? And the same instruction in μ C 8051? Distinguish between these two cases.

$PART - B (5 \times 16 = 80)$

- 11. Along with external hardware circuit and the machine cross-sectional diagram, explain how a stepper motor interface can be controlled from μ C 8051. Use the port-1 of μ C 8051. Assuming variable reluctance type stepper motor is available with a step angle of 2 degrees, write a program using 8051 assembly language for deflecting the stepper motor shaft by 30 degrees. Assume half-step mode.
- 12. a) i) Draw the timing diagram showing fetching and complete execution of the μP 8085 instruction MVI B, 9A_H. Assume that this instruction is fetched from memory location 4567_H.
 - ii) Along with a neat sketch of the functional block diagram / architecture, describe the salient features available in the 8-bit µP 8085. (8 + 8)

OR

b) i) Write a subroutine for generating a time delay in µP 8085, using software delay loop. Also evaluate the count required to obtain a time delay of about 15 msec. Assume a µP clock frequency of 3 MHz.