End Semester Examinations - Nov/Dec 2012 (R 2008)

BE(Full Time) – III Semester- Electrical and Electronics Engineering

College of Engineering, Anna University,Chennai-600 025

Time : 3 Hours | EE 9204- Digital System Design | Max Marks :100

Answer ALL Questions

Part –A **10 X 2 = 20**

1. Add $(2096)_{10}$ to 01101101011101110 using Hexa decimal arithmetic.
2. Use De Morgan's rules to show that a two input NOR gate with inverted inputs acts like an AND gate.
3. Use a Karnaugh map to minimise F = AB' + C'D + C + B'C'D
4. (i) A ROM has 12 address lines . Calculate the number of memory locations. (ii) A 64 bit square memory matrix is addressed by the binary number 110100. In which row and in which column is the wanted location.
5. Use a 2 X 4 PAL and implement the logic function F = AB + A'B' .
6. Construct a divide by 16 ripple up counter.
7. What is a Merger diagram? What are its uses?
8. Implement the function F(x1,x2,x3,x4)== $\sum$ (0,1,3,4,8,9,15) with an 8X1 multiplexer where the following variables are connected in the specified order to the selection lines s2,s1,s0 x1,x3,x4.
9. Investigate the transition table of Figure -1 and determine all critical and non critical race conditions.

$Y_1 y_2$	$X_1 X_2$ 00	01	11	10
00	10	00	11	10
01	01	00	10	10
11	01	00	11	11
10	11	00	10	10

Figure -1

10. What are FPGAs ? Mention few applications of FPGAs.

Part-B **5 x 16 =80**

11. (i) Convert the number $[700]_8$ to base 4, base 12, base 16 and base 32 (4)

(ii) Design a minimal two level gate combinational network that detects the presence of any of the six invalid code groups in 2421 code by providing a logic 1 output. Realize using NAND gates (8)

(iii) Detect and correct the error (if any) in the following even parity Hamming coded message. 1100111 (4)

12 ((i) A logic circuit is required in which the output is HIGH if the input A is HIGH together with either input B or C but not both OR if all three inputs are low.

(a) Write down the truth table for the circuit (3)

(b) Write down the reduced Boolean equation that describes the circuit (2)

(c) Draw the logic diagram (3)

(ii) Use a Karnaugh map to simplify F = AB'C + A'B'C' + A'B'C+AB'C'+ABC. Implement the reduced expression using NAND gates. (8)

(OR)

12(b) (i) Design a combinational circuit that multiplies two 2-bit numbers a_1a_0 and b_1b_0. Use AND gates and half adders for realisation. (8)

(ii) Using the Quine- Mccluskey method obtain all the prime implicants and the essential prime implicants of the given Boolean function . Draw the logic diagram for the reduced expression $F(x1,x2,x3,x4) = \sum (1,4,6,7.8.9.10,11,15)$ (8)

13(a) (i) Given a 16 x 16 ROM chip with an enable input. Show the external connections necessary to construct a 64 x 16 ROM with four chips and a decoder (4)

(ii) Construct a 5X32 decoder with four 3 x 8 decoders with enable inputs and one 2 x 4 decoder (4)

(iii) Draw a ROM to implement the Boolean functions

$F_1 = ABCD+AB'CD'+ A'BC'D+ABC'D'$

$F_2 = AB'+A'B$ (8)

(OR)

13(b) (i) Realize the functions given below using a PLA. Give the PLA table and internal connection diagram for the PLA:

$F1(a,b,c,d) = \sum m(1,2,4,5,6,8,10,12,14)$