BE/B.Tech(Full Time),DEGREE END SEMESTER EXAMINATION,NOV/DEC 2011

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGG

THIRD SEMESTER (REGULATIONS 2004)

COLLEGE OF ENGINEERING, ANNA UNIVERSITY,CHENNAI-600 025

(R 2004)

Time : 3 Hours EE 273- Digital System Design Max Marks :100

Answer ALL Questions

Part-A (10 x 2 =20 Mark)

1. Perform the subtraction using r's complement arithmetic.
   (i) $(0234)_{12}$-$(0089)_{12}$ (ii) $(0FE3)_{16}$-$(0FF0)_{16}$
2. Write the eight bit signed magnitude, two's complement, one's complement representations for each decimal number. (a) +120 (b) -42
3. Evaluate: {(a+b'+c) +(b+c')+ (a'+b')+(a'+b'+c')}'.
4. Convert the Boolean Expression f(A,B,C) = AB + C into SOP form
5. Construct a logic network for the function H = (x .y)'.z' using only NOR gates.
6. Implement the following four variable Boolean function using four input multiplexers and NAND gates. f(A,B,C,D) = Σm(0,7,8,9,10,11,15) Use B and C as control variables.
7. Give the truth table and excitation table of T Flip Flop.
8. Draw the circuit diagram of three bit up counting ripple counter
9. Differentiate combinational and sequential circuits.
10. What is meant by fundamental mode operation of an asynchronous circuit?

Part-B (5 x 16 =80 Mark)

11.

(i) Convert the number $[\,700\,]_8$ to base 4, base 12, base 16 and base 32 (4)

(ii) Detect and correct the error in the following even parity Hamming coded message. 1001001 (4)

(iii) What are reflecting codes ? . Give examples. (4)

(iv) Perform the BCD subtraction $(0456)_{10}$- $(0234)_a$ and XS3 addition $(0902)_{10}$ + $(0283)_{10}$ (4)

12. a) (i) Design a full bit adder circuit. (8)

(ii) Reduce the Boolean function F(x1,x2,x3,x4)=– $\sum$ (0,2,3,4,8,10,12,13,14) using Karnaugh map and implement using gates. (8)

(OR)

12(b) (i) Using the Quine- Mccluskey method obtain all the prime implicants and the essential

prime implicants of the given Boolean function . Draw the logic diagram for the reduced expression using NOR gates. F(x1,x2,x3,x4)== $\sum$ (0,1,2,12,13,14,15) (12)

(ii) Give the truth table for a multiplier that multiplies two two bit numbers. (4)

13(a) (i) What are the functional blocks available in a memory chip ? Draw the diagram . (4)

(ii) Given a 64x4 ROM chip with an enable input. Show the external connections necessary to construct a 128 x 8 ROM with four chips and a decoder. (6)

(iii) What is a multiplexer? Show the internal connections for a 8 x 1 Multiplexer (6)

(OR)

13(b) Realize a BCD to seven segment code converter using PLA. Also give the PLA table and show the connection diagram. (16)

14 (a)(i) For the sequential network shown in figure-1 (16)

derive the state table and draw the state diagram . What is the function of the circuit?

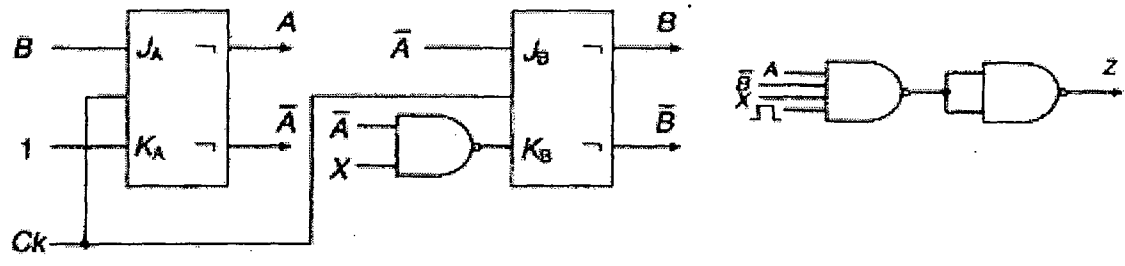

Figure 1

(OR)

14.b) Design a synchronous counter that goes through the sequence ... 1-2-4-5-7-10-13-15-1..

Use T FFs for implementation. (16)

15.(a) Draw the general block diagram of an asynchronous circuit and explain the functioning of the circuit.

(OR)

15.(b) Design a gated latch with two inputs x_1 and x_2 and one output z. The inputs never change simultaneously . Th output is to be the same as x_1 if x_2=1 .However if x_2=0 the output is to remain fixed at its last value before x_2 become zero. Use SR latches for realisation.