Dept. of ECE, CEG Campus, Anna University
End Semester Examinations Apr-May 2011
B.E.(ECE) VIII Semester (FT, Regular)
EC525 – RF System Design
Answer All Questions

Part A (10x2=20 Marks)

Q1. It is required to deliver 250mW to a 50 ohm load at 1GHz. But the driving power amplifier can only support a maximum of 2Volts at its output. Design any one L matching network to be inserted between power amplifier and the 50 ohm load.

Q2. Explain how you would distinguish between homodyne and heterodyne receiver architectures.

Q3. Explain when you would prefer a pi matching network over an L matching network.

Q4. What is the origin of drain current noise in a MOSFET, and how is it modeled (give equation and equivalent circuit).

Q5. Given an amplifier with its equivalent input noise specified in terms Vn and In, what is the optimum source impedance for this case (to obtain a minimum Noise Figure).

Q6. The VCO is modeled in terms of K_{VCO}. Give the appropriate equation connecting the input and output, explain what each term represents, and give the units for K_{VCO}.

Q7. Using a suitable sketch, indicate all the possible leakage paths in a mixer and name them appropriately.

Q8. Fig.1 shows a ring oscillator. Indicate the phase of the oscillating signal at the output of each stage. The bubble indicates 180^0 phase difference between input and output of the corresponding buffer.

Q9. Fig.2 illustrates one problem associated with the down-conversion of an RF signal using a non ideal LO signal. Explain in brief what this problem is.

Q10. Fig.3 below represents the root locus plot of a cross coupled LC oscillator. What do the small crosses, arrows and circle represent in this diagram.

Part B (16x5 = 80Marks)

Q11. Consider the GPS receiver RF front shown below in Fig. 4.You may note that the data pertaining to each stage is given either above or below each stage. In Fig.1, 'IL' means insertion loss, and 'conversion gain' refers to the gain of the mixer.

(a) What is the total Noise Figure of this system (only upto the input of the VGA stage) (4)

(b) Assuming that the signal power picked up the antenna is -130dBm, what is the power level at each stage of the chain (upto input of VGA). (6)

(c) Assuming 50 ohm antenna impedance, what is the Noise power (dBm) at each stage of the chain (upto VGA input). Give the answers to part (b) and (c) in the form of a table. (6)

(Fig.4 is taken from a paper from German Space Agency DLR, published in the April 2011 issue of IEEE MTT)

Q12a. Consider the Colpitts oscillator and its equivalent circuit shown below in Fig.5a and Fig.5b respectively.

(i) Unlike the usual case, why is the current source pointing upwards in this case. (3)

(ii) V_{xout} is shown across a resistor whose value is not shown. Give the expression or value of this resistor (3)

(iii) Obtain an expression for the transondcutance 'gm' so that the system is capable of oscillating.(10)

OR

Q12b. For a nonlinear amplifier, consider the input output relation between v_i and v_o. as given below

$$v_o = c_0 + c_1 v_i + c_2 v_i^2 + c_3 v_i^3 + \ldots$$

(i) Give the expression for IM3, the third order inter-modulation ratio. (3)

(ii) Deduce the relation between IM3, IIP3 and Pin and indicate the units of these quantities in the resulting equation. (4)

(iii) Show that the input voltage corresponding to the IIP3 point is given by (3)

$$V_{i,IP3}(dB) = 20\log\left(\left|\frac{c_1}{c_3}\right|\right) + 10\log\left(\frac{4}{3}\right)$$

(iv) What is the corresponding relation between the $V_{o,IP3}$ and the coefficients c_1, c_3 etc.(5)

(v) Deduce the following relation between 1dB compression and the third order intercept point. State whether the variables in this equation refer to the values at the input or at the output. Comment on whether the units indicated in this equation are correct. (5)

$$\mathbf{P1dB} = IP3 - 9.6dB$$

Q13a. (i) Fig 6. below shows part of the RF front end of a receiver. The 'I' channel mixer alone for is shown in the figure, with a similar diagram to be used for the Q channel mixer. Explain the principle of operation of the mixer used in this circuit.(6). *(Fig.6 is taken from a MIMO receiver paper by Razavi, appearing in IEEE JSSC 2007)*

(ii) Explain how the circuit shown in Fig. 7 works like a mixer. Explain the main drawback of this mixer.(6)

(iii) The inductors and the tank circuit in the Gilbert cell mixers shown in Fig.8 are introduced to overcome (or atleast reduce) certain drawbacks. Explain how what these drawbacks are and how they overcome(or reduced).(4)

OR

Q13b. An LC oscillator along with an equivalent circuit are shown below in Fig.9a and Fig.9b.

(i) Write down the expression for Z(s) shown in the equivalent circuit.(4)

(ii) Draw the circuit corresponding to the V to I block shown in the equivalent circuit. What is the transfer function of this block.(4)

(iii) Write down the expression for the loop gain and obtain the expression for the poles of the transfer function.(8)

Q14a. (i) Derive the expression for the transfer function of a multiplier used as a Phase Detector(PD). If this is used as part of a PLL, under locked condition, comment, with justification, on the phase relation between the two inputs of the PD.(4)

(ii) For the phase frequency detector shown in Fig.10, sketch the waveforms for the U and D signals for any assumed input (V) and reference (R) signals. How does this scheme get used as phase detector and obtain an expression for Kpd, the conversion gain of the phase detector. Draw the circuit of the charge pump to be used with this circuit and give the expression for the conversion gain of the charge pump.(4+4)

OR

Q14 b. Consider the equivalent block diagram of a PLL shown in Fig.11. Write down the expressions for the transfer function $\Phi_o(s)/\Phi_i(s)$. Give the corresponding (transfer function) expression involving frequencies. Consider different cases of Z(s) to show that the system can be (i) unconditionally stable, (ii) unconditionally unstable and (iii) conditionally stable. (3+3+10).

Q15.a(i). Consider the Class D power amplifier shown in Fig.12. Sketch the V_{DS} and I_D waveforms for M1. Also show the corresponding waveforms across the load resistor R_L. What can be the maximum possible efficiency for this scheme and how can this be obtained (or approached) in practice. (3+3+2)

(ii) For the Class F power amplifier shown in Fig.13, sketch the waveforms for V_{DS} and I_D of the MOSFET. Explain the need for the quarter wave transmission line in this scheme. (3+5)

OR

Q15b (i). In this question, you have to calculate the Phase Noise specification for the LO. For GSM standard, the receiver sensitivity is -99dBm, required SNR is 9dB, BW is 200KHz. Consider a -43dBm blocker at a located at 600KHz offset from the required RX signal. Fig.14a below (left depicts) the spectrum of the required signal(small delta function), blocker (bigger delta function) and LO spectrum with its phase noise. Fig.14b shows the spectrum after down conversion. In order to meet the required SNR calculate the permissible phase noise of the LO at 600KHz offset from the carrier. Your answer must be in units of dBC/Hz @600KHz. For your calculation, you can assume that the LO phase noise at 600Khz offset is approximately flat over a 200Khz band. (8)

(ii) Fig.15 below is part of a 3G RF front end stage. Sketch the possible waveforms for $\Phi1$, $\Phi2$,$\Phi3$,$\Phi4$ (exact time axis units not required, but relative phasing amongst them needed to show the concept involved). You need to consider only the mixer, and here, the mixer is labeled as HB (High Band) mixer, with an identical LB (Low Band) mixer not shown. (8) *(Fig.15 is from a paper from Sony-Ericcson, published in 2011 ISSCC Conf. Digest).*

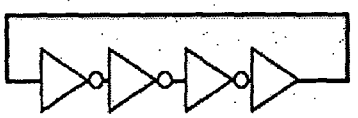

Fig.1

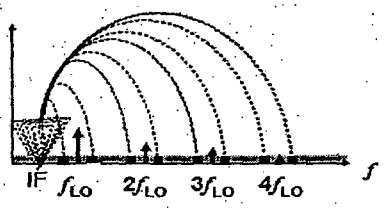

Fig.2

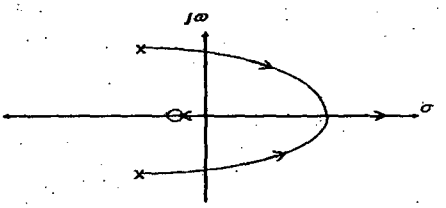

Fig.3

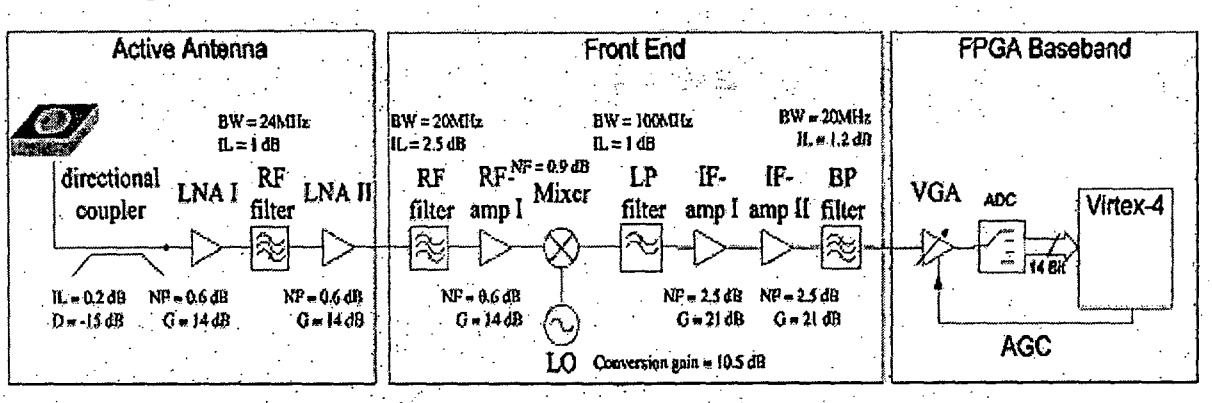

Fig.4

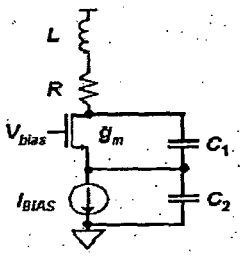

Fig.5a

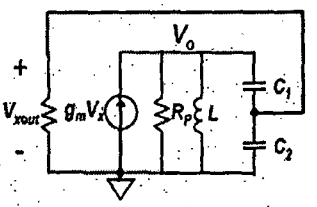

Fig.5b

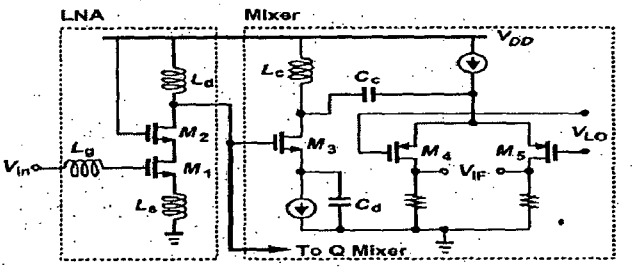

Fig.6

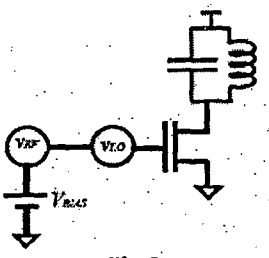

Fig.7

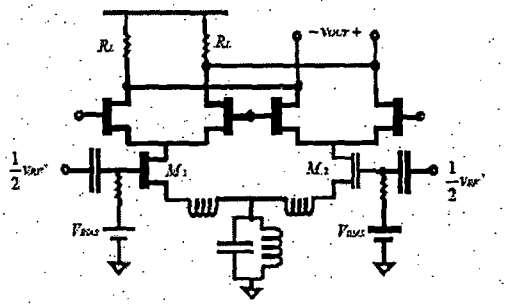

Fig.8

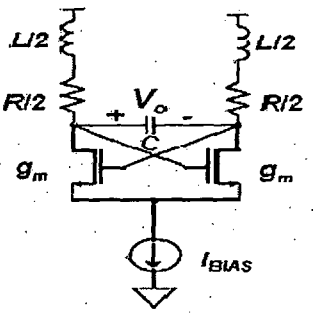

Fig.9a

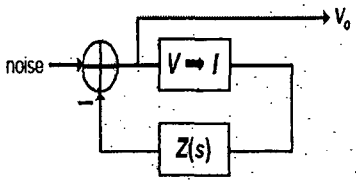

Fig.9b

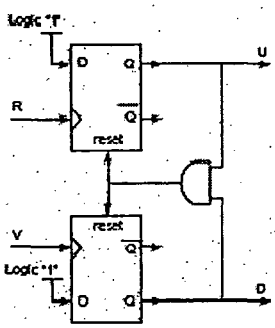

Fig.10

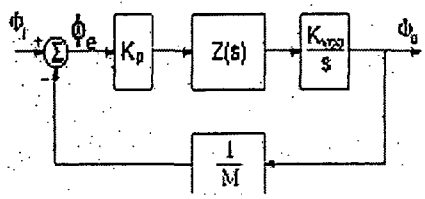

Fig.11

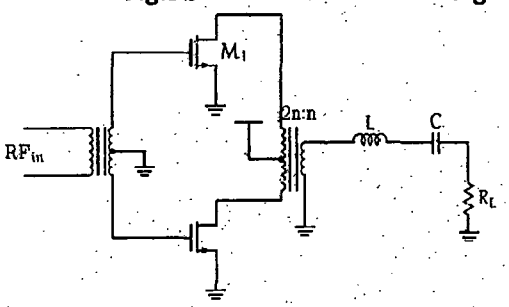

Fig.12

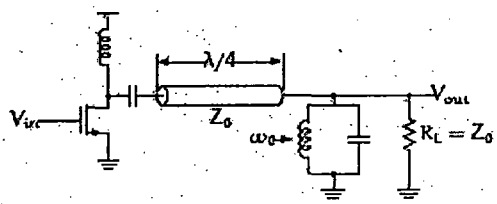

Fig.13

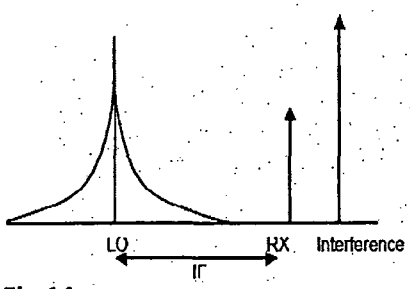

Fig.14a

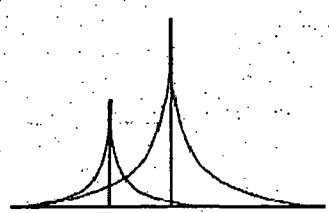

Fig.14b

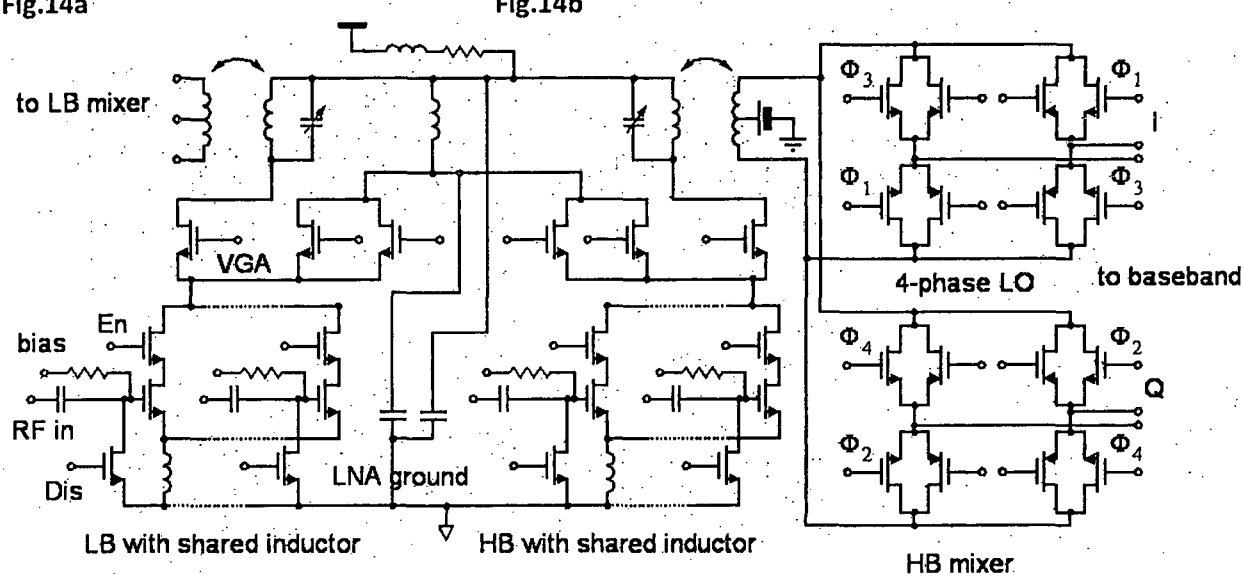

Fig.15