Roll No.									

DEGREE	:	B.E. (FULL TIME) DEGREE EXAMINATION
Branch	:	ELECTRONICS & COMMUNICATION ENGG.
Month & Year	:	APRIL / MAY 2011
Semester	:	EIGHT SEMESTER REGULATION 2004
Code No. / Subject	:	EC 514 – CAD for VLSI

Time: 3 Hours **Max. Marks: 100**

Answer All Questions

Part – A **10 x 2 = 20 Marks**

1. Define "data structure" and "algorithm". What are the basic operations performed on "data structures"
2. What are the different complexity classes of algorithm? Arrange them in the increasing order of time complexities.
3. What is meant by simulated Annealing?
4. List out the applications of compaction.
5. What do you infer from the Multi level logic Synthesis?
6. Define Channel Routing.
7. List the optimization problems related to floor planning.
8. Draw the Time-wheel implementation of event queue.
9. Define BDD.
10. The assignment problem itself consists of several sub problems. State any two?

PART- B **5 X 16 = 80 Marks**

11)

(a)

(i) Explain in detail about the physical design cycle. (8)

(ii) Explain how to perform "preorder" traversal for a binary tree. (8)

12)

(a) What is meant by "minimal spanning tree"? Explain the "Prim's" and "Kruskal's" algorithm to construct it. (16)

(or)

(b) With neat sketch, describe the Dijkstra's shortest path algorithm? (16)

13)

(a) With a neat sketch explain the different ways present in the incremental computation of a spanning tree. (16)

(or)

(b) Explain the following Algorithms in detail.

(i) Liao-Wong Compaction Algorithm. (12)

(ii) Bellman Ford Algorithm. (4)

14)

(a) Give a brief note on Kernighan-Lin partitioning algorithm. What are the steps involved in the application of Kernighan-Lin partitioning algorithm. (16)

(or)

(b) Compute the positive co-factor of an ROBDD. List out the various factors. (16)

15)

(a) With neat sketch explain gate level modeling simulation. (16)

(or)

(b) Describe the Force directed scheduling algorithm. (16)