B.E/B.Tech Degree End Semester Examinations, Apr/May 2011
Electronics and Communication Engg.
VII Semester – (Regulations : 2004)
EC-472 – VLSI Design

Time: 3 Hours | Answer ALL questions | Max.marks: 100

PART-A (10X2=20 marks)

1. What is the threshold voltage of MOS device?
2. What is the effect of gate capacitance and on resistance of MOS device by fixed voltage scaling?
3. Indicate the different symbols used for various regions in stick diagram.
4. What are the features of pass transistor logic?
5. Differentiate latch and register.
6. Draw the circuit of a dynamic RAM memory cell.
7. List different types of shifters.
8. What are the power minimization techniques used in datapath structures?
9. What are the different types of cell based design methodology?
10. Differentiate hard and soft macros.

PART-B (5X16=80 marks)

11. a. Derive an expression for drain current of a MOS transistor.
    b. Discuss the voltage transfer characteristics of CMOS inverter.

12. a. Implement a 4-input NAND gate using static CMOS and DCVSL logic.

    (or)

    b. Discuss the working principle and signal integrity issues in dynamic logic

13. a Explain the construction of master-slave edge triggered register with its timing properties.

    (or)

    b i. Briefly explain the impact of clock skew on the performance and functionality of synchronous design
    ii. Write short notes on Dual edge registers.

14. a Explain the operation of Manchester carry chain adder and find the worst case delay of carry chain.

    (or)

    b Explain the features of Modified Booth's recoding for multiplication with an example.

15. a i. Explain the steps involved in Semiconductor Design Flow. (6)
    ii. Write short notes on Array based implementation. (10)

    (or)

    b i. Explain briefly about array-based programmable wiring and switch box based programmable wiring.
    ii. Explain the architecture of any one type of FPGA.