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B.E/B.Tech (Full Time) DEGREE END SEMESTER EXAMINATIONS, APRIL/MAY 2011

ELECTRONICS AND COMMUNICATION ENGINEERING BRANCH

SIXTH SEMESTER

EC 9078 –EMBEDDED AND REAL TIME SYSTEMS

Duration : **3 Hrs** Max. Marks : **100**

Answer **ALL** Questions

PART-A **(10 x 2 = 20 Marks)**

1. What are the major levels of abstraction in the embedded design process.
2. Write the ARM assembly language program to implement the C program:

```
if (x<3) {      a = b*c;
         }
else     {      a = a + (b*c);
         }
```

3. Draw the UML state diagram of a bus bridge operation.
4. What is a "symbol table" and how it is built?
5. Draw the CDFG for the following code fragment:

```
for(i=0, f=0 ; i< N ; i++)
    f = f + c[i]*x[i];
```

6. Differentiate between a reentrant program and a non reentrant program with an example for each.
7. Write the equation for computing the total speedup S for a kernel when an accelerator is used.
8. Bring out the difference between fixed-priority arbitration and fair arbitration.
9. Draw the UML class diagram for the software modem.
10. What is meant by "feature creep"?

PART-B **(5 x 16 = 80 Marks)**

11.(i) With neat sketches, explain in detail about the direct mapped cache and the set associative cache. (8)

(ii) How could the pipeline throughput efficiency be improved?. Explain with an example ARM language program. (8)

12.(a)(i) Briefly explain the three important loop optimization techniques with an example for each. (10)

(ii) With neat sketches, explain the operation of touchscreen. (6)

(OR)

(P.T.O)

12.(b)(i) With an example, explain the domain testing for a pair of variables and the data flow testing in detail. (10)

(ii) For the basic block given below, obtain the single assignment form and also draw the DFG for that form

```
x = a + b;
y = c + d;
z = x + e;
```
(6)

13.(a)(i) Schedule the process given below using the Earliest Deadline First (EDF) scheduling policy. Compute the schedule for an interval equal to the least-common multiple of the periods of the processes. Assume the time starts at t=0.

Process	Execution Time	Period
P1	1	3
P2	1	4
P3	2	5

(10)

(ii) Write a brief note on preemptive multitasking. (6)

(OR)

13.(b)(i) What is the need to optimize the power for a process?. Explain the L-shaped usage distribution and the Advanced Configuration and Power Interface (ACPI) in detail. (8)

(ii) With neat sketches, explain why does the critical timing race occurs in shared memory communication and also suggest the methods to avoid the race condition. (8)

14.(a)(i) With neat sketches, briefly explain the typical bus transactions that take place on the I^2C bus. (8)

(ii) With a block diagram, briefly explain how the CPU cache can cause problems for an accelerator and also suggest a technique by which the problem could be overcome. (8)

(OR)

14.(b)(i) With neat sketches, explain about the Ethernet and also bring out the difference between Ethernet and Myrinet. (8)

(ii) With an example, explain how does a single threaded control and multithreaded control of an accelerator will affect the speedup factor. (8)

15.(a)(i) Write a brief note on "System on Silicon". (6)

(ii) With neat block diagrams, explain the hardware architecture and software architecture of a set-top box. (10)

(OR)

15.(b) With neat sketches, explain the entire design of data compressor based on Huffman coding principle. Also illustrate the Huffman coding with an numerical example. (16)