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B.E. / B.Tech. (Part Time) DEGREE END SEMESTER EXAMINATIONS, APRIL / MAY 2014

ELECTRONICS AND COMMUNICATION ENGINEERING BRANCH

Sixth Semester

PTEC9255 - COMPUTER ARCHITECTURE AND ORGANIZATION

(Regulations :2009)

Duration: 3 Hrs. **Maximum Marks 100**

Answer All Questions

Part A **10 X 2 = 20 Marks.**

1 Write down the IEEE 754 standard 32 bit floating point number format

2 List out few major register level component types

3 Draw a full adder circuit using two level logic

4 What is guard bits? Where is it used?

5 List out any two advantages of hardwired control over micro-programmed control

6 What is superscalar processing?

7 What are the advantages of optical memories?

8 List out any four types of semiconductor memories

9 How does microprocessor responds to the DMA request and when is it honoured by the processor?

10 List out any four differences between RISC and CISC processors

Part B **5 X 16 = 80 Marks.**

11 i) Briefly explain different types of instruction formats with an example (8 marks)

ii) List out different addressing modes available and give example (8 marks)

12 a) Explain modified booth algorithm and illustrate with an example

(or)

b) How do you perform floating point addition? Illustrate with an example and also explain how pipeline can be applied

13 a) i) What are the differences between classical and one hot method? explain (4 marks)

ii) Illustrate and implement the Control unit of GCD processor using classical method (12 marks)

(or)

b) i) Briefly discuss about instruction pipeline (6 Marks)

ii) Write in detail of nano-programming and its advantages and disadvantages over microprogramming (10 marks)

14 a) i) List out different ways to allocate the memory and explain each one (8 marks)

ii) What are the different replacement policy available and compare each one (8 marks)

(or)

b) i) What is cache memory? How do you compare this memory with other memories? (8 marks)

ii) Design a four way set associative cache with the following parameters: the capacity of the cache is 64KB; the cache block size is 32 B and the width of the system data bus is 32 bits (8 marks)

15 a) i) Explain with neat diagram the different types of bus arbitration (8 marks)

ii) Write a short notes on PCI interrupt and vector interrupts (8 marks)

(or)

b) Briefly discuss the following

i) Multiprocessors (6 marks)

ii) Fault tolerance (5 marks)

iii) Vector processor (5 marks)