Dept. of ECE, CEG Campus, Anna University
End Semester Examinations Apr-May 2014
B.E.(ECE) VI Semester (FT, Regular)
EC9075 CMOS Analog Design I
Answer All Questions

Part A (10x2=20 Marks)

Q1. Sketch Vx versus Ix for the circuit in Fig.1 below. Assume that the capacitor is initially discharged.

Q2. Determine the expression for the small signal gain of the circuit shown in Fig.2.

Q3. Give the expression for the differential gain of the circuit shown in Fig.3 Assume λ is zero for all transistors.

Q4. Give the expression for the gain of the circuit given Fig4

Q5. What is the mean square value of the output short circuit noise current for the circuit shown in Fig5.

Q6. Consider any differential amplifier and explain what is meant by input offset voltage.

Q7. If it is required to reduce the output impedance and also reduce the input impedance of an amplifier, what type of feedback will you use.

Q8. In negative feedback system, what are the implications of having a phase margin close less than 45^0.

Q9. Explain why common mode feedback is required.

Q10. Give the noise equivalent circuit of a MOSFET.

Part B (16x5=80)

Q11a What is the feedback topology used in the diagram in Fig.6. What are the units for the gain of the forward amplifier and gain of the feedback network. What should be the ideal values of Rout and Rin. (2+4+2)

Q11b Consider the amplifier shown in Fig.7. Cut the feedback loop anywhere and determine the expressions for the loop gain, input impedance and output impedance. Ignore loading effect. (3+3+2)

Q12a. Give the expression for the differential gain for the circuit in Fig.8. Give the expression for the output impedance of this circuit. (12+4)

OR

Q12b. Determine the small signal gain of circuit shown in Fig.9.

Q13a. In Fig.10, the transistors M3 (NMOS) and M4 (PMOS) are biased in the linear region to act as a resistors. This circuit can be used as a Variable Gain Amplifier for AGC purposes in wireless communication. Explain how this circuit can operate as a Variable Gain Amplifier and give an expression for its small signal gain. (8+8)

OR

Q13b. Study Fig.11a, and Fig.11b carefully and then answer the following questions. Identify the input and output waveforms in each case. Indicate if each of the four waveforms is a current waveform or a voltage waveform. In the region indicated by the arrow (1) in Fig.11b, give the possible expression for the slope of the waveform. (4+4+8)

Q14a. Study the Fig.12 carefully and label the transistors. Assume that the Enable and Disable transistors are used as ideal on-off switches. Assume '0' and 'V_{DD}' as the supply voltages. Suggest values for Enable and Disable for the overall amplifier to be either in the 'On' condition or in the OFF condition. Give the expression for the small signal differential gain of the system. Is this a single 'stage' or two 'stage' amplifier. Explain the principle of operation of CMFB in this circuit. (2+8+2+4)

OR

Q14b. Study the circuit in Fig. Q13 carefully. This circuit makes use folded cascade, gain boosting and possible pole zero cancellation. Explain each of these principles and utility, and identify the locations/regions in the diagram where these principles are utilized. (4+4+4+4)

Q15a. Give the small signal equivalent circuit and determine the transfer function of the circuit shown in Fig. 14 and give the expressions for its poles and zeros. (2+8+6)

OR

Q15b . Draw the half circuit equivalent for the common mode and true differential and true common inputs to the circuit in Fig. 15. Assuming λ=0 for M7, what is the expression for the differential gain of the circuit. Assuming λ finite, M7 what is the expression for common gain of this circuit. Also, give an expression for the minimum common mode input that can be applied while all the transistors are still in saturation.

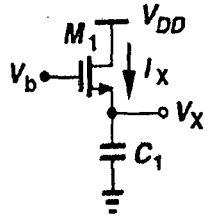

Fig.1

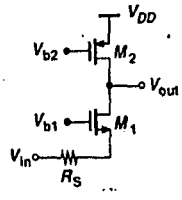

Fig.2

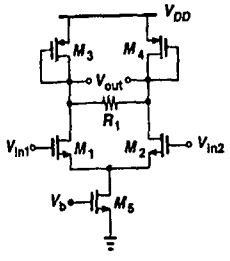

Fig.3

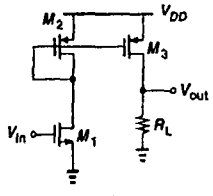

Fig.4

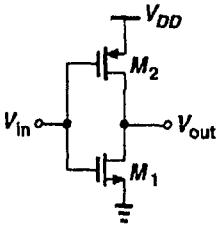

Fig. 5

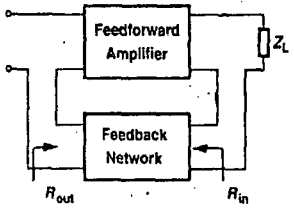

Fig.6

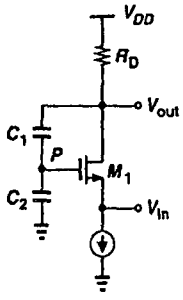

Fig.7

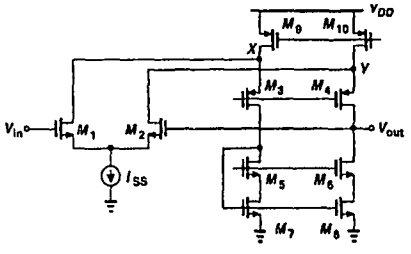

Fig.8

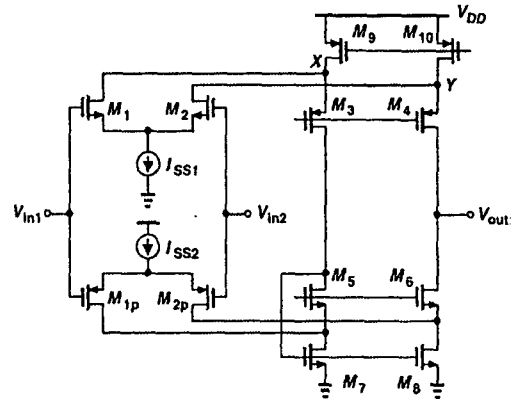

Fig.9

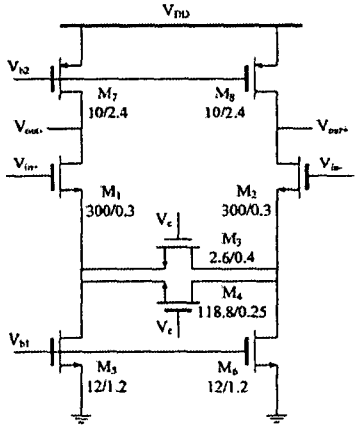

Fig.10

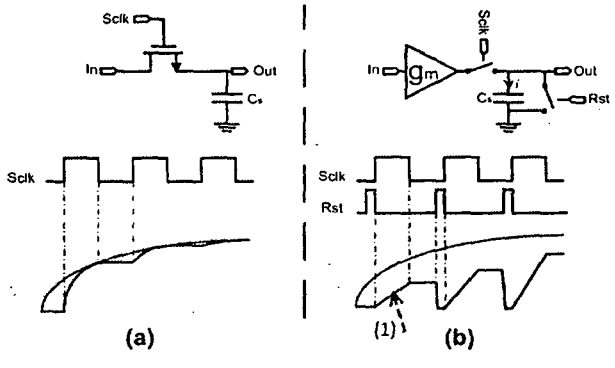

Fig.11

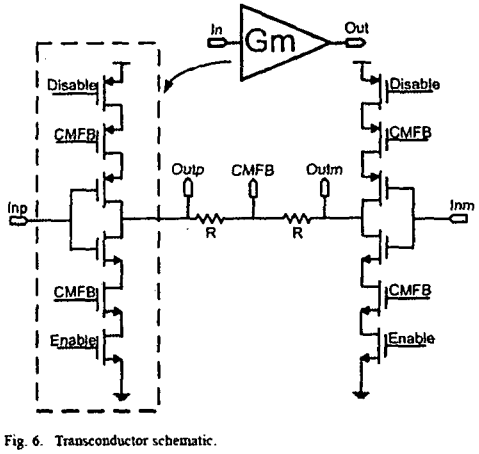

Fig. 6. Transconductor schematic.

Fig.Q12

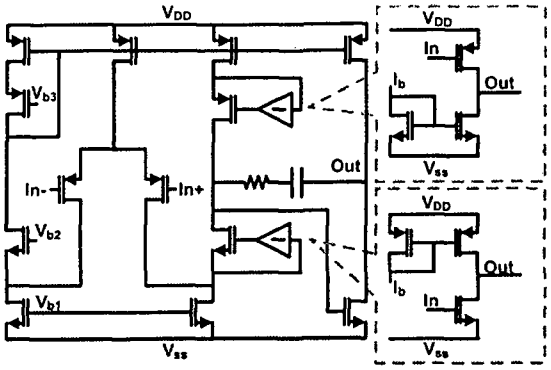

Fig. 13

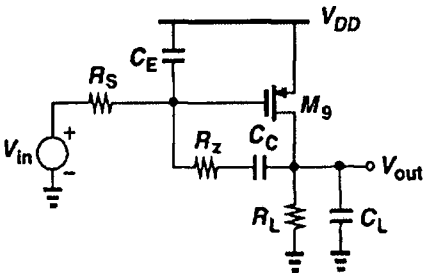

Fig. 14

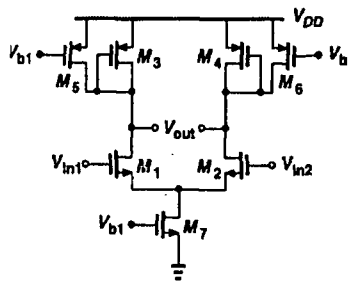

Fig.15