B.E. / B.Tech (Part Time) DEGREE END SEMESTER EXAMINATION APR/MAY 2014
Electronics and Communication Engineering Branch
V Semester - (Regulations 2005/2009)
PTEC472/PTEC 9355 – Digital VLSI

Time: 3 Hours **Max.marks: 100**
Answer ALL questions **PART-A** **(10X2=20 marks)**

Use following device parameters for calculations.
NMOS: $VTn_0 = 0.4$, $k'_n = 115\mu A/V^2$, $VDSAT = 0.6V$, $\lambda = 0.06V^{-1}$, $\gamma = 0.4\ V^{1/2}$, $2\Phi_F = -0.6V$
PMOS: $VTp_0 = -0.4V$, $k'_p = -30\mu A/V^2$, $VDSAT = -1V$, $\lambda = -0.1V^{-1}$, $\gamma = -0.4V^{1/2}$, $2\Phi_F = 0.6V$

1. Find the operating region of NMOS transistor with V_{GS}=2.5V, V_{DS}=1V, and V_t = 0.4V.
2. What is the effect on capacitance of MOS device due to fixed voltage scaling?
3. Draw the layout of two input NAND gate.
4. What is the voltage swing of NMOS pass transistor logic?
5. Differentiate latches and registers.
6. Draw the circuit of one transistor dynamic RAM cell.
7. What is a data path operator?
8. What is meant by clock skew in synchronous system?
9. Implement a two input AND gate using two input multiplexer.
10. What are the features of Full-custom design?

PART-B **(5X16=80 Marks)**

11. (i) Implement the Boolean logic Y = A'+ B'+ (CD)' using Static CMOS and Dynamic logic and size the devices such that the equivalent impedance is equal to inverter with size (W/L)p = 3/1 and (W/L)n = 1/1,.
(ii) Discuss the signal integrity issues of dynamic logic.

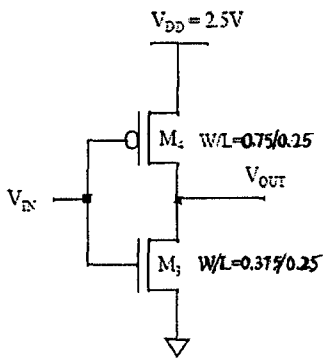

Figure 1

12.(a) The inverter in figure 1 operates with V_{DD} = 2.5V Find V_M, V_{OH}, V_{OL} and V_{out} for Vin = 0.9V.

(OR)

12.(b) i. Discuss the secondary effects of MOS device.
ii. Two MOSFETs fabricated in a long channel process (assume $\lambda = 0$) are tested and the measurements are given below. Both devices have W/L = 2.4μm/1.2μm. (V_{SB} = 0 in all cases): Determine the type of device, V_{T0} and k' for MOSFET A and B.

Condition:	$\|I_D\|$ - MOSFET A	$\|I_D\|$ - MOSFET B
VGS = 0V, VDS = 0V	0A	0A
VGS = -1V, VDS = -2V	20μA	0A
VGS = 1V, VDS = 1V	0A	45μA
VGS = 1V, VDS = 0.02V	0A	4μA
VGS = -2V, VDS = -2V	200μA	0A

13.(a) (i) Find the set-up and clock to output delay of MUX based edge triggered register.
(ii) Explain pipelining with an example.

(OR)

13.(b) (i) Show that C^2MOS register is insensitive to 0-0 overlap.
(ii) Explain the read and write operation of static RAM cell.

14.(a) Find the propagation delay of Manchestor carry chain adder and Carry bypass adder.

(OR)

(b) Find the critical path of 4 X 4 Wallace tree multiplier.

15.(a) Explain briefly about Cell based implementation.

(OR)

15.(b) Explain the architecture of any one type of FPGA.
