
COLLEGE OF ENGINEERING, ANNA UNIVERSITY
END SEMESTER EXAMINATIONS – April/May 2011
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
Fourth Semester
EC281 Digital Electronics and System Design
Regulation 2004

Time: 3 hours Max marks: 100

Part A (10x2=20 marks)

1. Convert the following Hex decimal number to octal and decimal number 92FF.7F
2. Express $a_1a_2 + a_2a_3$ as the product of maxterms
3. Explain propagation delay and noise margin
4. Draw two input NOR gate using RTL
5. Draw the circuit diagram for a full adder using half adder
6. Define priority encoder?
7. Write down the excitation table for RS flip flop
8. Differentiate between Moore and Mealy machine
9. Distinguish between synchronous and asynchronous circuit
10. Define critical race

Part B (5x16=80 marks)

11 i) State and prove De Morgan's theorem (6 marks)
ii) Using a Karnaugh map, determine the MSP and MPS forms of the switching function
$F = \sum(0,2,5,7,8,9,10,15) + \sum_{\varphi}(3,4)$ (10 marks)

12 a) i) Draw the circuit diagram and explain the operation of three input NAND gate using CMOS gate (8 marks)
ii) Draw the circuit diagram of CMOS inverter and explain its Operation (8 marks)

(or)

b) i) Explain with neat diagram and working of two input NAND gate using DTL (8 marks)
ii) Explain with neat circuit diagram the operation of open collector output using TTL families (8 marks)

13 a) i) Implement the following switching function using multiplexer

$F(w,x,y,z) = \sum(0,7,11,15) + \sum_{\varphi}(2,3,4,13)$ (8 marks)

ii) Implement the following function using PLA

i. $F_1(a,b,c) == \sum(0,1,2,3,6,7)$

ii) $F_2(a,b,c) == \sum(1,3,7)$ (8 marks)

(or)

b) Design a combinational circuit that converts a 8421 code to Excess 3 code

14 a) Minimize the following state table

	NS,Z			
PS	X_1X_2			
	00	01	11	10
A	A,0	C,1	F,0	G,1
B	B,0	D,1	F,0	H,1
C	C,0	G,0	H,0	F,1
D	D,0	A,0	B,0	F,1
E	E,0	B,0	H,0	F,1
F	F,0	E,1	A,1	H,0
G	G,0	E,1	F,0	B,1
H	H,0	D,1	F,0	A,1

(or)

b) Using T flip flop design a synchronous counter which counts in the following sequence: 000,010,011,101,110,111,000,010......

15 a) What are the different kinds of hazards present in the circuit? Explain with an example the elimination of hazards in the circuit

(or)

b) i) What is fundamental mode operation in asynchronous circuits? Explain (6 marks)

ii) The output z of a fundamental mode, two input sequential circuit is to change from 0 to 1 only when x_2 change from 0 to 1 while x_1 = 1. The output is to change from 1 to 0 only when x_1 changes from 1 to 0 while x_2 = 1.

a) Find a minimum row reduced flow table

b) Write a set of hazard free excitation and output equations

(10 marks)