B.E. DEGREE END SEMESTER EXAMINATIONS, APRIL / MAY 2014
ELECTRONICS AND COMMUNICATION ENGINEERING
FOURTH SEMESTER – (REGULATIONS 2008)
EC 9251 DIGITAL ELECTRONICS AND SYSTEM DESIGN

Time: 3 hr Max. Marks: 100

Answer ALL Questions

Part – A (10 x 2 = 20 Marks)

1. Convert (458.23) in decimal number system into its equivalent octal and hexadecimal code.
2. Realize f(A,B,C,D) = Σ(1,3,5,7,9,11,13,15) using appropriate MUX without extra gates.
3. Convert JK flip flop into D flip flop.
4. Draw the Moore state diagram to provide an output Z = 1, if the input sequence X is 010. The circuit never resets and overlapping is allowed.
5. What is race?.
6. Define static-1 and static-0 hazard.
7. Define fanout and noise margin..
8. What are the applications of an open-collector TTL gate.
9. Sketch the internal architecture of a PLA involving 3 variables.
10. Sketch the circuit of 1-bit SRAM cell.

Part – B (5 x 16 = 80 Marks)

11. Obtain simplified SOP using Quine-McClusky method for
F(A,B,C,D,E,F) = Σ(0,2,4,6,9,11, 13,15,17,21,25,27,29,31)

12(a). Design a BCD to seven segment decoder circuit. Assume don't cares.

OR

12(b). Derive the PLA programming table for the combination circuit that squares a 3 bit number. Minimize the number of product terms. Draw and explain its implementation.

13 (a). (i) Draw the circuit diagram of a Master-Slave JK FF and explain. (8)
(ii) Design a counter using JK FFs, with count sequence 0,2,4,6,1,3,5,7 and repeat. (8)

OR

13 (b). (i) Consider 4-bit Johnson counter with modification to prevent lock out. Assume the initial state to be 1010. Determine the next states of the counter till a valid state is reached. (6)

(ii) Reduce the Mealy table (10)

Present state	a	b	c	d	e	f	g	h
Nxt X = 0	c	d	h	b	e	f	c	c
State X = 1	f	c	e	a	c	b	h	a
Out X = 0	0	0	0	1	0	1	0	1
put X = 1	0	0	0	0	0	1	1	0

14 (a). Explain the problem of non critical and critical races in asynchronous sequential circuits with suitable examples.

OR

14 (b). Explain in detail the state development diagram and state assignment table in designing asynchronous sequential circuit with an example.

15 (a). With a neat diagram explain the working of tristate TTL gate.

OR

15 (b). i. Simplify and draw the logic diagram for the expression Y = C'B'A'+C'BA+CB'A using CMOS logic.

ii. Analyse the performance characteristics of TTL and CMOS logic.

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