B.E./B.Tech.(Full Time) DEGREE END SEMESTER EXAMINATIONS, April 2011

ELECTRONICS AND COMMUNICATION ENGINEERING

IV SEMESTER-(REGULATIONS 2009)

EC9255- COMPUTER ARCHITECTURE AND ORGANIZATION

Time -3 hours Total marks -100

Answer all questions

PART – A (10 X 2 = 20 Marks)

1. What are the fields in instruction format? How instruction format is optimized?
2. Construct a structural VHDL description of the full adder?
3. Write an expression for propagate-generate signals of carry look ahead adder.
4. Draw the architecture of full adder array for 4X4 bit unsigned multiplication?
5. Give an example of a processor where hardwired control design is used .why?
6. Draw the micro programmed control unit for the twos complement multiplier?
7. List the differences between SRAM and DRAM?
8. How many memory locations can be identified with sixteen address lines?
9. Compare and contrast RISC and CISC?
10. What do you mean by superscalar processor?

PART – B (5*16 = 80 Marks)

11. i)Describe any four addressing modes with examples. (8)
ii) Discuss the floating point representation for a single and double precision? (8)

12) A) Obtain HDL description for Booth multiplication algorithm and multiply 01100011 & 01010101. (16)

OR

B) Draw the data path of a sequential n-bit binary division. How non restoring division is superior to restoring division. Explain non restoring division with an example 1100 0010 /1010. (16)

13. A) Design the control unit of GCD Processor using one hot method. (16)

OR

B) Design a micro programmed control unit for the twos complement multiplier? (16)

14. A) Explain memory address translation architecture used in Intel Pentium Processor. (16)

OR

B) Explain any three methods of Cache mapping. (16)

15. A) Discuss and Analyze the three bus arbitration methods with respect to communication reliability in the event of hardware failures. (16)

OR.

B) What is DMA ?Why it is used. Draw the architecture of DMA controller. Explain its operation in different modes. (16)