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B.E / B.Tech (Full Time) DEGREE END SEMESTER EXAMINATIONS, NOV / DEC 2012

Electronics and Communication Engineering
III Semester
EC9202 – Electronic Circuits I
(Regulation 2009)

Time : 3 Hours | Answer ALL Questions | Max. Marks 100

PART-A (10 x 2 = 20 Marks)

1. Define CMRR of a differential amplifier.

2. What is the design consideration that has to be met to maintain thermal stability of BJT self Bias circuit.

3. Write the drain Current expression of NMOS, operating in triode region.

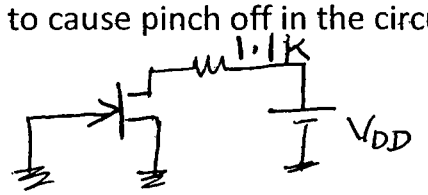
4. Define the critical Voltages VIL and VIH of a Logic inverter.

5. A Common base amplifier has maximum gain of 125 and R_{in} is approximately equal to 26 Ω . Find the Value of R_C . [$R_L = \infty$ and $R_S = 0$]

6. Briefly write about class D power amplifier.

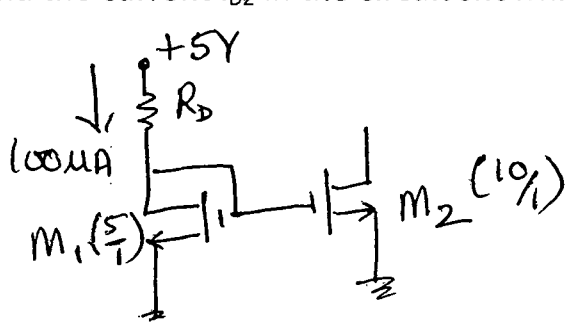
7. Draw CMOS Common drain amplifier with PMOS driver and depletion NMOS as active load.

8. Calculate the minimum Value of V_{DD} required to cause pinch off in the circuit shown. I_{DSS} = 10mA and V_{GS}= -4V



9. In a CE amplifier , R_E =2K is fully bypassed with C_e =4.7μf. Calculate the lower cut –off frequency due to CE [Assume gian = 24.4 mA/V].

10. Find the current I_{D2} in the circuit shown.

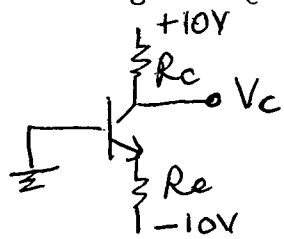


Part – B (5 x 16 = 80 marks)

11(i) Draw a Darlington amplifier and its equivalent circuit. Derive for A_{VS} , A_{IS}, R_{IN} and R_O. **(10)**

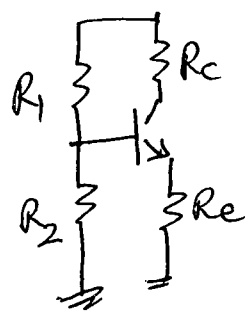
(ii) Design a single stage CE amplifier with gain of -29 using Fixed Bias with V_{CC} = 15v and R_L = 10K. & I_{CQ} =0.5mA and h_{fe} =100 **(6)**

12(a)(i) Design the Circuit given : I_C =1.5mA, V_C=4V and h_{fe}=100



(6)

ii) For the biasing circuit shown , derive expressions for the stability factors S , S' and S"



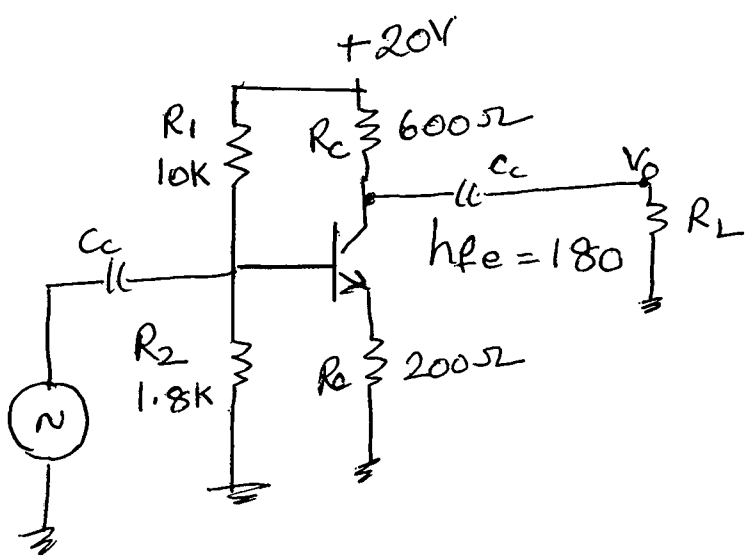
(10)

(OR)

(b) (i) Explain circuits using diodes to compensate for the changes in I_{CO} and V_{BE}

(8)

(ii) For the Circuit given find the maximum peak to peak signal when R_L = 1·2K



(8)

13 (a)(i) Draw a MOS differential amplifier with PMOS current source as active load and derive for its A_d and A_C with equivalent circuit. **(10)**

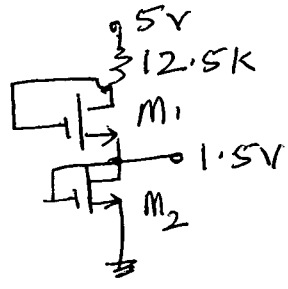
(ii)Draw a Current steering circuit with one sink and one source terminal. Write the expressions for all the terminal currents in terms of the reference current. **(6)**

(OR)

(b) (i) Draw a CMOS common source amplifier without feedback with NMOS driver and PMOS diode as active load **(10)**

- with equivalent circuit of active load derive for its offered resistance
- with equivalent circuit of driver ,derive for the Voltage gain.

ii) Calculate width of the devices M_1 and M_2 , Given $L_1 = L_2 = 1\ \mu m$ and $I_D = 120\mu A$ $\mu_n C_o = 180\mu A/V^2$ $V_{tn} = 1V$ and $\lambda = 0$ **(6)**



14(a) (i)Draw a discrete Common drain amplifier, with its equivalent Circuit derive for its A_V , R_{IN} and R_O. **(8)**

(ii) Draw the Voltage transfer curve of CMOS inverter function indicating the five regions of operation **(4)**

(iii) Determine the region of operation of CMOS inverter, when $V_{in} = 1.1$ V justify your answer. Assume $V_{DD} = 2.5V$, $V_{tn} = 0.5$, $V_{tp} = -0.5$ **(4)**

(OR)

(b) (i) With Voltage transfer Curve of NMOS inverter. Derive expressions for Noise margin in High and Low states. **(8)**

(ii) Design an NMOS inverter with maximum power dissipation = 0.5mW $\mu_n C_o = 25\ \mu A/V^2$ and $V_{DD} = 5V$. $V_T = 0.8V$. Draw the load line and mark the operating point in cut –off and triode regions. **(8)**

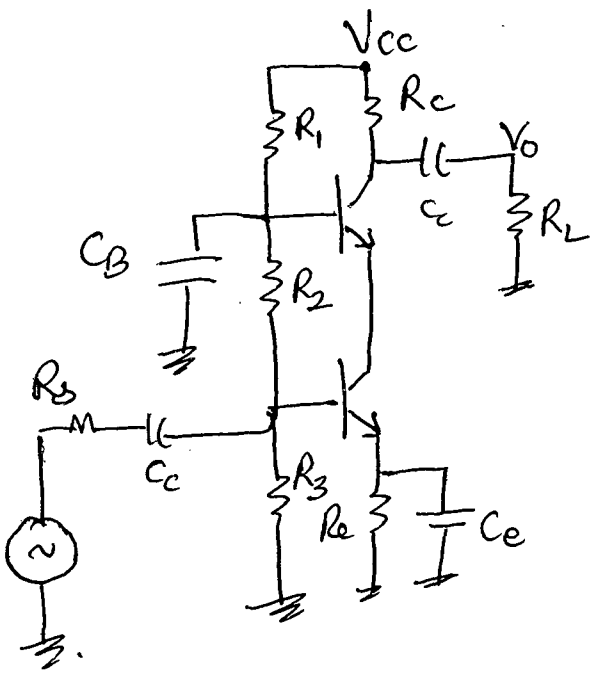
15(a) (i) Explain class B power amplifier and derive for its efficiency **(10)**

(ii) Design a class A transformer coupled power amplifier to deliver ac power of 5 watts to a load of 300Ω at 30% efficiency. Find ac power across the load and power dissipation. Also draw the designed circuit. Assume V_{CC} =20V and h_{fe} = 60 **(6)**

(OR)

15.(b) (i)Define and derive for f_α and f_β. **(8)**

(ii)For the Circuit shown calculate the midband gain and effective higher cut –off frequency. **(8)**



R_C=9K hfe =100 (both Trs)

R_E=1K hie =5.2k

R_1=125K Cb'e=35pf

R_2=50K Cb'c =4pf

R_3 =26K

R_S =100Ω **(8)**

R_L= 90K