BE/BTECH (FT-arrear) DEGREE END SEMESTER EXAMINATIONS APR/MAY-2014
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
III SEMESTER
EC8301 ELECTRONIC CIRCUITS-I
(Regulation 2012)

Time:3Hrs **Max Marks:100**

Answer all questions

Part-A (10 X 2=20 Marks)

1) Compare Fixed-bias, Collector-to-base bias and Voltage divider bias of BJT biasing methods.

2) Compare between JFET and MOSFET amplifiers

3) Calculate the small-signal voltage gain of the bipolar transistor circuit shown in Figure 1.

Assume the transistor and circuit parameters are β=100, V_{CC}=12V, V_{BE}=0.7V, R_C=6kΩ,

R_B=50kΩ and V_{BB}=1.2V.

4) Define CMRR of BJT differential amplifier. How to improve it?

5) Determine the input impedance of CG amplifier

6) Compare Common-Source, Common-Drain and Common-Gate Amplifiers based on their characteristics.

7) Compare between NMOS inverter with enhancement, depletion and resistive load

8) Draw the small signal circuit diagram of CMOS Common source amplifier

9) What is the relationship between f_β and f_α

10) Define Miller effect

Part-B (5 X 16=80 Marks)

11) i) Explain Current-steering Circuit in detail (8)

ii)Determine the differential voltage gain, common-mode voltage gain and CMRR of the CMOS differential amplifier as shown in Figure 2. The transistor parameters are Kn=100μA/V^2, Kp=50μA/V^2,Vtn=0.8V, $(W/L)_{NMOS}$=15, $(W/L)_{PMOS}$=30, Vtp=-0.6V, I_D=200μA λn=0.01V^{-1}, λp=0.008V^{-1} and minimum overdrive voltage of 0.3V is required to operate all transistors in the saturation region. (8)

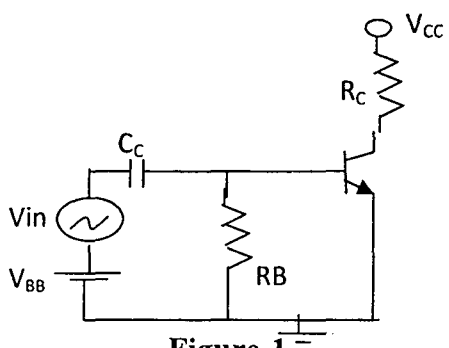

Figure-1

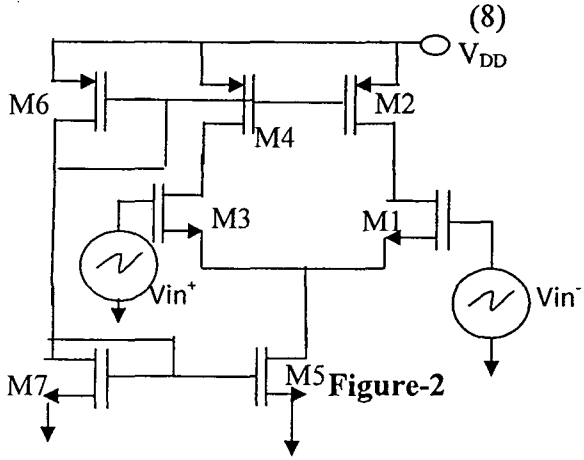

Figure-2

12)a) Determine the change in collector current produced in each bias referred to in example Figure 3. When the circuit temperature raised from 25°C to 105°C and I_{CBO} =15nA @ 25°C (16)

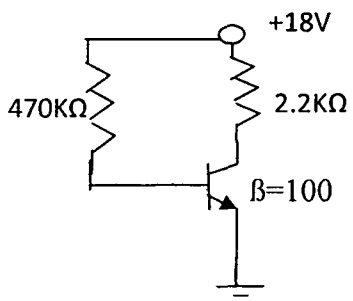

Figure-3(a)

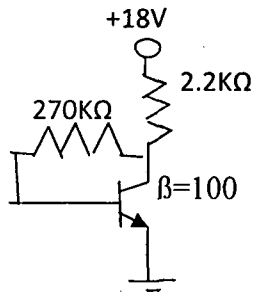

Figure-3(b)

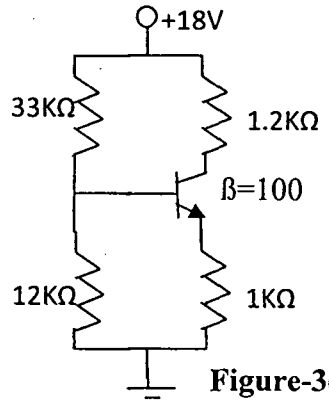

Figure-3(c)

(OR)

b)(i) Calculate the drain current and source-to-drain voltage of a Common-source Circuit with P-channel enhancement mode MOSFET shown in Figure 4. Let Vtp=-0.8V and βp=0.4mA/V^2 (8)

ii)Define and derive the stability factors for BJT self bias (voltage-divider bias) circuit. (8)

13)a) i) For each transistor in the Darlington circuit shown in Figure 5 has the parameters of β=100, V_A=∞. Determine its overall voltage gain, input impedance and output impedance. (8)

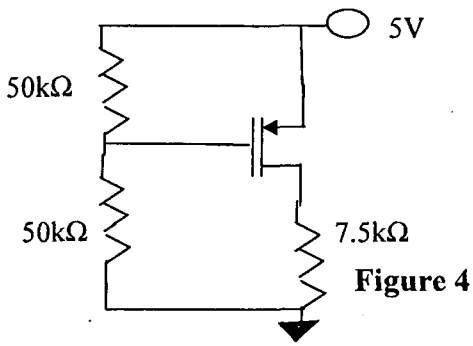

Figure 4

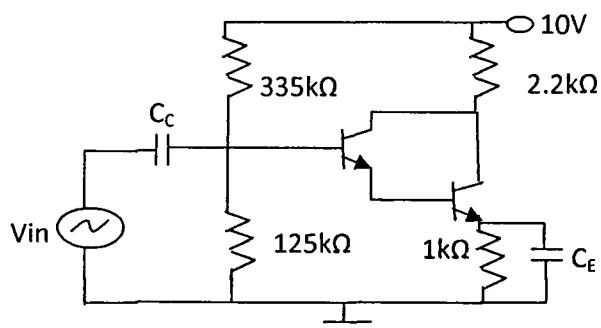

Figure 5

(ii) Determine the small signal voltage gain, input impedance and output impedance of cascode amplifier. (8)

(OR)

b) For the circuit in Figure 6, the parameters are R_B=100kΩ, R_E=10kΩ, R_C=10kΩ, V_{CC}=V_{EE}=10V, R_L=1kΩ, R_S=1kΩ, β=125 and V_A=∞. (w)Determine the small signal voltage gain (x) Determine small signal current gain (y)Determine the input resistance, Rin (z) Determine the output resistance, Ro. (16)

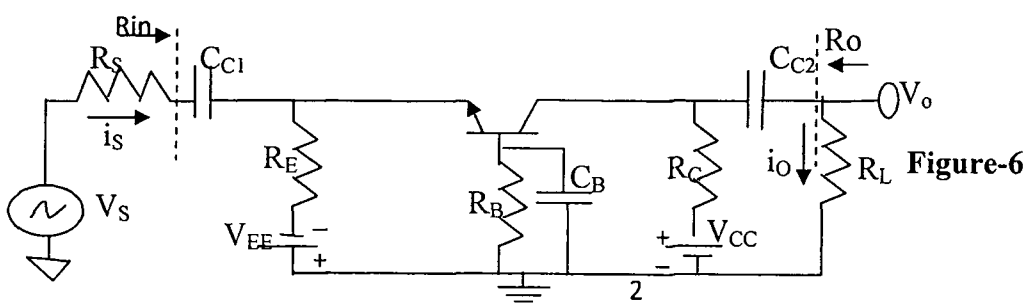

Figure-6

14(a) i) Determine the Voltage gain, input impedance and output impedance of BIMOS amplifier (8)

(ii) Consider the circuit shown in Figure 7 with circuit parameters V^+=5V, V^-=-5V, Rs=4kΩ, R_D=4kΩ R_L=4kΩ and R_G=50kΩ. The transistor parameters are Vtp=-0.8V, βp=2mA/V^2 and λ=0. Draw the small signal equivalent circuit, determine the small signal voltage gain, input impedance and output impedance. (8)

(OR)

b)i) Determine the voltage gain and input impedance of JFET Common source amplifier (8)

ii) The transistor in the source-follower circuit shown in Figure 8 is biased with a constant current source. The transistor parameters Vtn=2V, Kn=40μA/V^2 and λ=0.01V^{-1}. The load resistor R_L=4 kΩ. (x) Design the transistor width-to-length ratio such that gm=2mA/V when I=0.8mA. What is the correspondence value for V_{GS}=? (y) Determine the small-signal voltage gain and output impedance. (8)

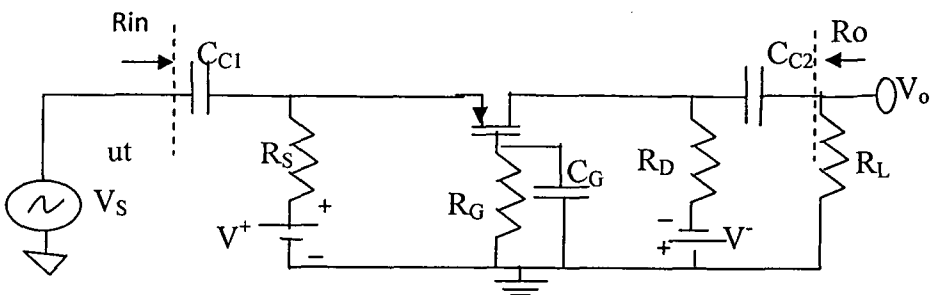

Figure-7

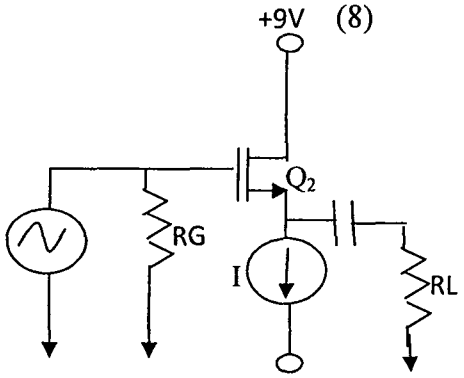

Figure 8

15)a) Determine the Midband gain, Upper Cutoff frequency of a Common-Source amplifier fed with the signal having internal resistance Rsig=100kΩ. The amplifier has RG=4.7MΩ, RD=RL=15kΩ, gm=1mA/V, ro=150kΩ, Cgs=1pF and Cgd=0.4pF. Also find the values of CC1,CC2 and CS by assuming lower cutoff frequency of 100Hz and that the nearest break frequency be atleast a decade lower.(vide Figure 9) (16)

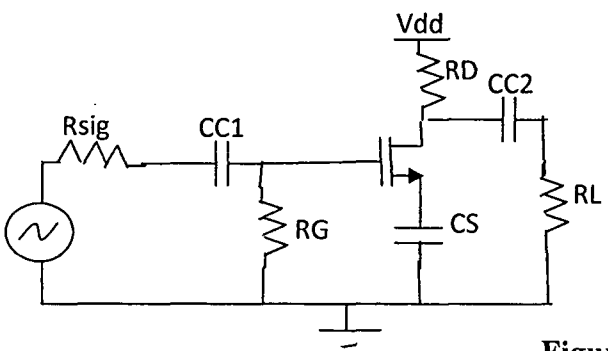

Figure 9

(OR)

b)i) Determine mid-band gain and upper cut-off frequency of Common Emitter amplifier (8)

ii) Determine mid-band gain and upper cut-off frequency of Common Source amplifier (8)