BE/BTECH (FT-arrear) DEGREE END SEMESTER EXAMINATIONS APR/MAY-2014
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
III SEMESTER
EC9202 ELECTRONIC CIRCUITS-I
(Regulation 2008)

Dur:3Hrs **Max Marks:100**

Answer all questions

Part-A (10 X 2=20 Marks)

1) Draw the DC load line of the circuit shown in Figure 1.

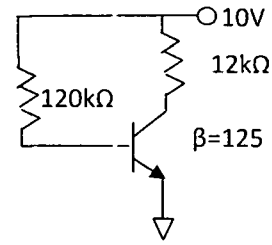

Figure-1

2) What is the role of bypass capacitor in BJT CE-amplifier circuit?

3) Determine the input impedance of common base amplifier.

4) Define CMRR. How to improve it.

5) Compare Common-Source, Common-Drain and Common-Gate Amplifiers based on their characteristics.

6) Draw the Voltage transfer characteristics of CMOS inverter for $\beta n/\beta p=0.1$, $\beta n/\beta p=1$ and $\beta n/\beta p=10$

7) Compare NMOS inverter with enhancement, depletion and resistive load.

8) Draw the small signal model of the CMOS common-source follower amplifier.

9) Find the unity gain bandwidth of MOSFET whose g_m=6mA/V, C_{gs}=8pF, C_{gd}=4pF and C_{ds}= 1pF.

10) Define cross-over distortion. How to overcome it.

Part-B (5 X 16=80 Marks)

11) (i) For the circuit shown in Figure 2, let $V_{DD}=V_{SS}$=1.5V, Vtn=0.6V, Vtp=-0.6V, all channel lengths=1μm, Kn=200μA/V^2, Kp=80μA/V^2 and λ=0. For Iref=10 μA, Find the widths of all transistors to obtain I_2=60μA, I_3=20μA and I_5=80μA. It is further required that the voltage at the drain of Q2 be allowed to go down within 0.2V of the negative supply and voltage at the drain of Q5 be allowed to go up to within 0.2V of the positive supply. (8)

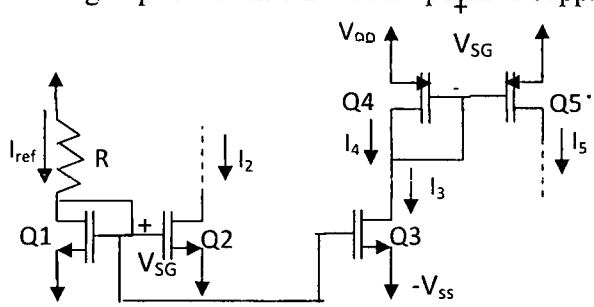

Figure-2

ii) Determine the differential voltage gain, common-mode voltage gain and CMRR of the CMOS differential amplifier. (8)

12)a) Determine the change in collector current produced in each bias referred to in example Figure 3. When the circuit temperature raised from 25°C to 105°C and I_{CBO} =15nA @ 25°C (16)

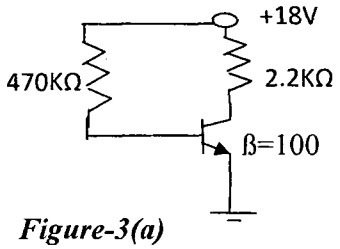

Figure-3(a)

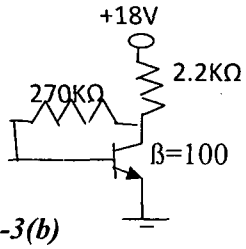

Figure-3(b)

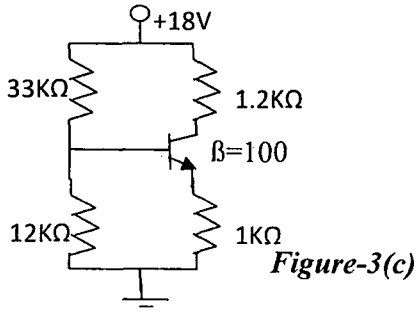

Figure-3(c)

(OR)

b) i)Define and derive the stability factors for BJT self bias (voltage-divider bias) circuit. (10)
ii) Determine the quiescent current and voltage values in a p-channel JFET circuit (Figure-4). (6)

13)a)i)Determine the Voltage gain, Current gain, Input Impedance and Output Impedance of Darlington pair amplifier. (8)
ii) Determine the Voltage gain, Input Impedance and Output Impedance of Common-Base amplifier. (8)

(OR)

b)i) Determine the Voltage gain, Input Impedance and Output Impedance of Cascode Amplifier.
ii) Determine the voltage gain, input impedance and output impedance of CE amplifier (8+8)

14)a) Explain the DC characteristics of a CMOS inverter with necessary diagrams and derivations. (16)

(OR)

(b)(i) Consider the circuit shown in Figure 5 with circuit parameters V^+=5V, V^-=-5V, Rs=4kΩ, R_D=4kΩ R_L=4kΩ and R_G=50kΩ. The transistor parameters are Vtp=-0.8V, βp=2mA/V^2 and λ=0. Draw the small signal equivalent circuit, determine the small signal voltage gain, input impedance and output impedance. (8)
ii) Determine the voltage gain, current gain, input impedance and output impedance of source degenerator (MOSFET configuration). (8)

15)a) Determine the voltage gain, input impedance, output impedance and bandwidth of the multistage amplifier. (16)

(OR)

b)i) Explain Class AB Power amplifier using MOSFET as output stage (8)
ii) Calculate the actual efficiency of the Class A output stage. Consider the common-source circuit in Figure 6. The circuit parameters are V_{DD}=10V, R_D=5kΩ, βn=2mA/V^2, Vtn=1V and λ=0. Assume the output voltage swing is limited to the range between the transition point and V_{DS}=9V to minimize the nonlinear distortion (8)

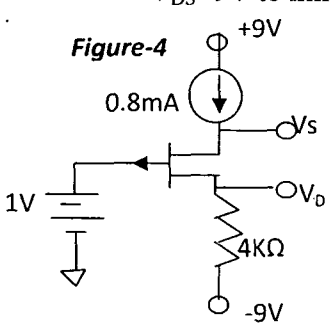

Figure-4

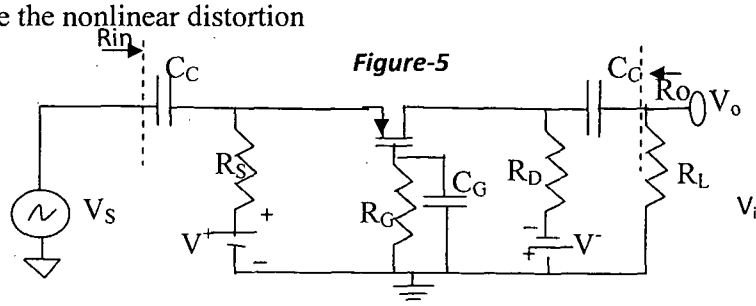

Figure-5

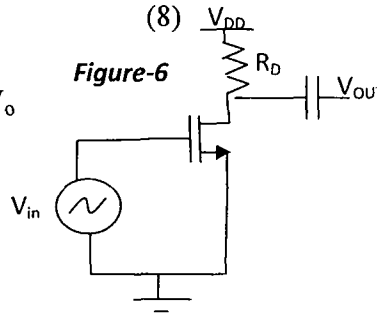

Figure-6