Roll NO									

B.E. / B.Tech. (Full Time) DEGREE END SEMESTER EXAMINATIONS, APRIL / MAY 2014

ELECTRONICS AND COMMUNICATION ENGINEERING BRANCH

Third Semester Bio-Medical Engineering

EC 9251 DIGITAL ELECTRONICS AND SYSTEM DESIGN

(Regulations :2008)

Duration: 3 Hrs. **Maximum Marks 100**

Answer All Questions

Part A **10 X 2 = 20 Marks**

1 Simplify the following expression

(BC'+A'D)(AB'+CD')

2 Draw a full adder circuit using half adder

3 What is the difference between Moore and Mealy machine

4 Write down the characteristic equation and excitation table for RS flip flop

5 Define critical race and how do you overcome this

6 Define fundamental mode of operation

7 What are the advantages of static RAM over dynamic RAM?

8 Implement the following function using ROM

$f(w,x,y)=\Sigma(2,3,7)$

9 Define noise margin

10 What are the advantages of CMOS logic over TTL logic?

Part B **5 X 16 = 80 Marks**

11 Reduce the following function using Quine McCluskey method

$f(A,B,C,D,E,F) = \Sigma_m (1,2,3,16,17,18,19,26,32,39,48,63) + \Sigma_d (15,28,29,30)$

12 a) Design a 3 bit counter which counts in the sequence

001,011,010,110,111,101,100,001,..... using J K flip flop

(or)

b) Reduce the following state table to a minimum number of states

Present state	Next state		Output	
	x=0	x=1	x=0	x=1
a	h	c	1	0
b	c	d	0	1
c	h	b	0	0
d	f	h	0	0
e	c	f	0	1
f	f	g	0	0
g	g	c	1	0
h	a	c	1	0

13 a) i) What is hazard? How do you take care of static and dynamic hazards? (8 marks)

ii) Briefly discuss about Essential hazards (8 marks)

(or)

b) An asynchronous sequential network is designed to capture pulses on an input line X. The network has a single input X, a reset input R and an output Z. If X changes from 0 to 1 or from 1 to 0 while R is 0, then the output Z becomes 1 and remains 1 until the network is reset. Thus, if there is a pulse on the input line when R is 0, the output will becomes 1 to indicate the occurrence of the pulse. When R=1, Z=0. Find a minimum row flow table

14 a) Realize the following function using PLA

$f_1(a,b,c,d) = \Sigma(4,5,10,11,12)$

$f_2(a,b,c,d) = \Sigma(0,1,3,4,8,11)$

$f_3(a,b,c,d) = \Sigma(0,4,10,12,14)$

(or)

b) i) What is CLB? Explain its function using circuit diagram (10 marks)

ii) How is programmable inter connect are useful for the interconnection? briefly explain (6 marks)

15 a) What are the advantages of dynamic CMOS over static CMOS? Explain with neat diagram three input NAND and three input NOR gate realization using static CMOS

(or)

b) i) Explain with circuit diagram the operation of Totem Pole TTL gate (8 marks)

ii) Explain with neat circuit diagram the operation of three state TTL gate (8 marks)