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B. E. / B.Tech. (FT) DEGREE END SEMESTER EXAMINATIONS, APRIL / MAY 2014

COMPUTER SCIENCE AND ENGINEERING

III SEMESTER

CS 8301 COMPUTER ARCHITECTURE

(Regulations 2012)

Time: Three Hours Answer All Questions Max. Marks: 100

PART - A (10 X 2 = 20 Marks)

1. There are two options available to enhance the performance of a machine. One is to add a vector mode of computation that is 20 times faster than the normal mode of execution, which is used 60% of the time. Another is to double the clock frequency. Which of the two would be better?

2. State the CPU performance equation & discuss the factors that affect performance.

3. Distinguish between hardwired and microprogrammed control.

4. Identify the dependences in the following code snippet:
   ADD R1, R2, R3
   DIV R4, R1, R5
   ADD R5, R7, R4
   AND R5, R4, R2

5. What is a re-order buffer? How is it useful?

6. What is meant by dynamic scheduling?

7. Discuss the concept of a Booth's multiplier.

8. Give the basic cell of an array multiplier.

9. Show how a 32MB main memory can be realized using 32KB memory chips.

10. List down the functions to be performed by a serial I/O interface.

PART- B (5 x 16 = 80 Marks)

11. (i) Discuss in detail the various factors that need to be considered while designing the ISA of a processor. (10)

(ii) Discuss the basic operations that a processor has to perform to execute the following instructions: (6)

- MUL R1, [5000], #data – assume R1 is the destination
- BEQ R1, R2, disp – Branch on equal

12. a. (i) Discuss the implementation of the MIPS integer pipeline. (10)

(ii) What are the complications to be handled in a floating point pipeline? (6)

OR

b. (i)
```
LOOP  LD    R1, 30 (R2)
      SUB   R4, R6, R5
      ADD   R6, R7, R1
      AND   R9,  R6, R2
      JZ    R9,  LOOP
      ADD   R10,R1, R2
```
Indicate and discuss about the hazards that might occur in the 5-stage MIPS pipeline.
Show the timing diagram for the above sequence assuming data forwarding is not supported. (10)

(ii) What is meant by forwarding? How is it handled in MIPS? (6)

13. a. (i) Consider the following code and assume that the multiply instruction has a latency of 5, the divide instruction a latency of 10 and the add instruction a latency of 3. Also assume that there are separate functional units for effective address calculations, for ALU operations, and for branch condition evaluation. For a **speculative** processor, create a table showing when each instruction issues, executes, writes the result and commits, for one iteration of the loop and for atleast two instructions from the second iteration. Assume one CDB and that only one instruction can commit per clock cycle.

(10)

```
loop: LD     F0, 0(R1)
      ADDD   F0, F0, F2
      LD     F4, 0(R2)
      MULD   F0, F0, F4
      DIVD   F0, F0, F6
      SD     0(R2), F0
      DADDUI R1, R1, #8
      DADDUI R2, R2, #8
      DSGTUI R3, R1, R2 (test if done)
      BNEZ   R3, loop
```

(ii) What are multiple issue processors? Discuss briefly. (6)

OR

b. (i) What are control hazards? Discuss the different ways of handling them. (10)

(ii) Discuss any three techniques that the compiler uses to exploit ILP. (6)

14. a. (i) Discuss the organization of a sequential binary multiplier. Simulate the multiplication algorithm for the numbers 9 and 10. (10)

(ii) Discuss the IEEE format for representing floating point numbers. (6)

OR

b. (i) Discuss the non-restoring division algorithm. Simulate the same for the numbers 14 / 4. (10)

(ii) Discuss the concept of a carry look ahead adder. (6)

15. a. (i) Compare and contrast the various mapping policies used in cache memories. (6+4)
Consider a series of address references given - 2, 3, 11, 16, 21, 13, 64 and 48. Assuming a direct mapped cache with 8 one-word blocks that is initially empty, label each reference in the list as a hit or a miss and show the final contents of the cache.

(ii) Discuss the concept of virtual memory. (6)

OR

b. (i) Explain the interrupt driven mode of data transfer and the DMA driven data transfer, elaborating on how they are accomplished and their relative merits and demerits. (10)

(ii) Compare and contrast memory-mapped I/O and I/O mapped I/O. (6)

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