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B. E. / B.Tech. (FT) DEGREE END SEMESTER EXAMINATIONS, APRIL / MAY 2014

COMPUTER SCIENCE AND ENGINEERING

II SEMESTER

CS 8201 DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Regulation 2012)

Time: Three Hours Answer All Questions Max. Marks: 100

PART - A (10 X 2 = 20 Marks)

1. Convert the hex number F3A2 to binary and octal.
2. Show that that the excess -3 code is self complementing.
3. Is the NAND function associative? Justify.
4. The main stairway in a block of flats has three switches for controlling the lights. Switch A is located at the top of the stairs, switch B is located halfway up the stairs and switch C is positioned at the bottom of the stairs. Design a combinational circuit to control the lights on the staircase.
5. Give the HDL description of a positive edge triggered JK flip flop.
6. Show how timing signals can be generated using a binary counter and a decoder.
7. What is an essential hazard?
8. Comment on the circuit whose transition table is shown below:

	x_1x_2 = 00	01	11	10
00	00	11	01	00
01	00	01	00	01
11	01	11	10	11
10	10	11	01	10

9. What is an FPGA?
10. Differentiate between a PLA and a PAL.

PART- B (5 x 16 = 80 Marks)

11. (i) Simplify $F(A,B,C,D) = \sum(1,2,3,5,6,7,10,11)$, $d(A,B,C,D) = \sum(9,12,15)$ using Karnaugh map. Draw the logic diagram using NAND gates only. (8)

(ii) Simplify the Boolean expression F (A, B, C, D) = B+BCD+B'CD+AB+A'B+B'C. Indicate the theorems used. (4)

(iii) Express the following function as a sum of minterms and as a product of maxterms: F (A,B,C,D) = B'D+A'D+BD. (4)

12. a) (i) Discuss the principle of operation of carry-look ahead adders. (10)
Design a 4-bit carry-look ahead adder and draw the circuit. Calculate the delay for generating s_3 and c_4.

(ii) Design a 3x3 binary multiplier circuit. (6)

(OR)

b) (i) Design a four-input priority encoder with the D_0 input having the highest priority and the D_3 input having the least priority. (10)

(ii) Write a Verilog HDL model for the priority encoder given above. (6)

13. a) (i) Design a counter with the following repeated binary sequence: 0, 1, 3, 5, 7, 0, ... Use J-K flip flops. (10)

(ii) Draw the circuit of a four-bit universal shift register and discuss its operation. (6)

(OR)

b) (i) Discuss the design of a 4-bit up/down binary ripple counter using T flip flops. (10)

(ii) Reduce the number of states in the following state table and tabulate the state table:

Present state	Next state		Output	
	x=0	x=1	x=0	x=1
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

Starting from state *a* and the input sequence 01100010001, determine the output sequence for the original state table and the reduced state table. Compare the results. (6)

14. a) For the two-input, two-output system, whose primitive flow table is shown below, perform the following: (4+2+2+2+6)
- Merge the flow table by finding all compatible pairs using an implication table
- Find the maximal compatibles through a merger diagram
- Find the minimal set of compatibles that covers all the states and is closed

- Do a race-free state assignment
- Design the circuit

	x_1x_2 = 00	01	11	10
1	1/00	2/00	- /- -	7/00
2	1/00	2/00	5/- 0	-/- -
3	1/-0	3/10	5/10	-/- -
4	1/0-	4/01	6/01	-/- -
5	-/- -	3/10	5/10	8/10
6	-/- -	4/01	6/01	9/01
7	1/00	-/- -	6/0-	7/00
8	1/-0	-/- -	5/10	8/10
9	1/0-	-/- -	6/01	9/01

(OR)

b) (i) An asynchronous sequential circuit is described by the excitation function

$$Y = x_1x_2' + (x_1 + x_2')y$$

and the output function z = y.

Draw the logic diagram of the circuit. (2)
Derive the transition table and output map. (4)
Obtain a flow table for the circuit. (2)
Describe the behavior of the circuit. (2)

(ii) What is a static hazard? Discuss with examples.
Find a circuit that has no static hazards and implements the Boolean function

$$F(A,B,C,D) = \sum(3,4,5,6,11,12,13,14,15)$$ (6)

15. a) (i) Give the logic diagram of a basic RAM cell and discuss.
Show how a 64K X 8 RAM can be constructed, indicating all the connections and the decoding logic required. Use two-dimensional decoding. (10)

(ii) A 12-bit Hamming code word containing 8 bits of data and 4 parity bits is read from memory. What was the original 8-bit data word that was written into memory, if the 12-bit word read out is as follows: (6)

1. 000011101010
2. 101110000110

(OR)

b) (i) Discuss the construction of a typical ROM. (10)
What are the different types of ROM?
Show how a ROM can be used to implement a combinational circuit that finds the nine's complement of a BCD digit.

(ii) Show how the following functions can be implemented using a PLA: (6)
F1 (A,B,C,D) = $\sum$2,3,6,7,11,15 and F2 (A,B,C,D) = $\sum$0,2,4,6,8,9,11,12,13,15

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