**(DEC 415)**

# B. Tech. DEGREE EXAMINATION, MAY - 2015

## (Examination at the end of Final Year)

### ELECTRONICS AND COMMUNICATION ENGG.

## Paper - V : VLSI Design

**Time : 3 Hours** **Maximum Marks : 75**

***Answer question No. 1 compulsory*** ***(15)***

***Answer ONE question from each unit*** ***(4 x 15 = 60)***

***1)*** a) What are the advantages of FPGAs?

b) Write the program structure of VHDL.

c) What are the advantages of BiCMOS Technology?

d) Draw the circuit diagram of CMOS inverter.

e) Write an ENTITY of 4X1 MUX in VHDL.

f) Write the expression for drain current in saturation region.

g) Define logic synthesis.

h) What is lithography technique?

i) Write scaling factor of Gate capacitance.

j) Compare CPLDs and FPGAs.

**Unit - I**

***2)*** a) Short notes on advanced CMOS fabrication technologies.

b) Write a short note on following :

i) Figure of merit

ii) Pass transistor

OR

***3)*** a) Explain various regions of CMOS inverter transfer characteristics.

b) Write short note Latch up in CMOS ciruts.

**Unit – II**

***4)*** a) Draw the layout for NMOS inverter circuit.

b) Write short note wiring capacitances.

OR

***5)*** a) Draw the stick diagram and layout of CMOS 2 input NOR gate.

b) Explain Lambda (λ) based design rules.

**Unit – III**

***6)*** a) Construct an 8-bit Carry select adder Using adders and multiplexers.

b) Draw the schematic and logic diagram for a single bit adder and explain its Operation with truth table.

OR

***7)*** a) Compare the different types of CMOS subsystem Multipliers.

b) Design logic for an ALU that can perform both logical and arithmetic operations.

**Unit – IV**

***8)*** a) Implement of full adder using PLA.

b) Describe behavioral design elements with examples.

OR

***9)*** a) Explain about anti fuses used in FPGAs.

b) Write a program in VHDL for an 2X4 Decoder in behavioral and structural style.

**κβκβ**