# B. Tech DEGREE EXAMINATION, MAY - 2015 <br> (Examination at the end of Second Year) 

# Electronics \& Communications <br> Paper - V : DIGITAL ELECTRONICS 

## Time : 3 Hours

Answer question No. 1 compulsory $(15 \times 1=15)$<br>Answer ONE question from each unit

1) a) What is meant by radix (base) of number system?
b) What is Excess- 3 code?
c) What is meant by weighted number system?
d) Explain about race-around condition \& How to avoid it?
e) Which logic gate is used to compare the I/PS?
f) Express the function in $y=\mathrm{A}+\overline{\mathrm{B}} \mathrm{C}$ in canonical sop form.
g) What are the universal gates \& why they are called universal gates.
h) How many Half adders are used to construct full adder.
i) What is difference between combinational circuit \& sequential circuit.
j) What does 'ECC' stands for?
k) List the applications of shift register.
2) $(\mathrm{ECE})_{16}$ convert into Decimal number.
m) $(1001101)_{2}$ convert into Gray code.
n) Which code is called as self complementary code? Explain with example.
o) What is decoder?

## UNIT - I

2) a) Convert the (732) $)_{10}$ into Binary, octal \& Hexadecimal form.
b) Perform subtraction operation on 68-48 using 2' complement subtraction method.

## OR

3) a) Simplify the Boolean function by using K-map

$$
\mathrm{F}=\Sigma \mathrm{m}(0,1,2,5,7,9,12,13,15)
$$

b) Simplify the given Boolean function by using tabulation method

$$
\mathrm{F}=\Sigma \mathrm{m}(1,2,3,5,6,7,8,9,12,13,15)
$$

## UNIT - II

4) a) Draw \& Explain the operation of 4-bit parallel Adder.
b) Differences between serial adder \& parallel adder.

## OR

5) a) Design Encoder logic diagram to convert decimal number into Binary number.
b) What is multiplexer? Draw \& explain the operation of 8:1 mux.

## UNIT - III

6) a) Explain the operation \& Truth table of SR NAND latch.
b) Explain the operation of JK flip-flop.

## OR

7) a) Design MOD-10 Asynchronous counter using JK flip-flop \& Draw o/p waveforms.
b) Difference between synchronous \& Asynchronous counters.
8) a) Draw the PAL circuit to implement the logic functions listed below.

$$
\begin{aligned}
& \mathrm{A}(x, y, z)=\Sigma(1,2,3,4) \\
& \mathrm{B}(x, y, z)=\Sigma(0,1,6,7) \\
& \mathrm{C}(x, y, z)=\Sigma(2,6) \\
& \mathrm{D}(x, y, z)=\Sigma(1,2,3,5,7)
\end{aligned}
$$

b) Discuss the comparision between PROM, PLA, PAL.

## OR

9) Briefly Explain about the following logic families
a) RTL
b) DTL
c) TTL
d) ECL

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