(DCS 213)

B. Tech. DEGREE EXAMINATION, MAY - 2015

(Examination at the end of Second Year)

Computer Science

Paper - III : DIGITAL LOGIC DESIGN

Time : 3 Hours **Maximum Marks : 75**

Answer question No. 1 compulsory ***(15 x 1 = 15)***

Answer ONE question from each unit ***(4 x 15 = 60)***

1) a) Draw the truth table of NAND gate.

b) Design subtractor circuit.

c) Define positive logic of TTL family.

d) Define Decoder.

e) Define flipflop.

f) Draw 4×1 multiplexer.

g) Difference between ROM & RAM.

h) Define shift register.

i) What are universal gates?

j) What is sequential circuit?

k) What is state table?

l) State De Morgan's theorem.

m) What is combinational logic circuit.

n) What is BCD Code?

o) Difference between Asynchronous and Synchronous Circuit.

Unit – I

2) a) Convert the following :

i) $(3456)_{10}$ to base 2

ii) $(12EF)_{16}$ to base 8

iii) $(10110011)_2$ to base 16

iv) $(726)_8$ to base 10

b) Realize AND, OR, NOT, XOR gates using universal gates.

OR

3) a) Minimise the function using K-map and obtain minimal Sop function?

$f(A, B, C, D) = \pi (1, 2, 3, 4, 6, 9, 10, 12, + 14) + d (5, 7, 11)$

b) What are universal gates? Why they called so?

Unit – II

4) a) Draw and explain the operation of 4 bit comparator.

b) List the applications of multiplexers and demultiplexers.

OR

5) a) What is an encoder? Explain octal to binary encoder.

b) Design the full adder using two half adders and logic gates.

Unit – III

6) Explain the following related to sequential circuit with suitable example.

a) State Diagram.

b) State Table.

c) State assignment.

OR

7) a) Distinguish between edge triggering and level triggering give examples.

b) Differences between Transition Table and Excitation Table.

Unit – IV

8) a) Draw the circuit diagram of 4 bit ring counter using D-flip flops and explain its operation with the help of bit pattern.

b) Discuss comparision between PROM, PLA and PAL.

OR

9) a) Explain different types of ROM generally used.

b) Explain programmable array logic.

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